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Speed and Thermal Reliability Study of Aggressively Scaled Low Power Nanoscale RTFF/REFF/SSPL D-flip Flops

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Abstract

In this SPICE simulation study, we systematically analyzed the speed and reliability performance of RTFF (Input-aware pre-charge retentive true single phase clocked flip-flop), REFF (Redundancy eliminated flip-flop) and SSPL (Self-shut off pulsed latch) D-flip flops (FFs) with 16 nm CMOS process with a V_{DD} range from 0.7 V to 1 V at wide operating temperature (27 °C to 107 °C). The RTFF, REFF and SSPL showcased a power consumption of 4.803/11.67/15.97/24.34 µW, 4.996/8.671/12.95/19.9 µW, and 3.746/7.762/14.62/26.22 µW, respectively at a V_{DD} of 0.7/0.8/0.9/1.0 V at 27 °C. Similarly, RTFF, REFF and SSPL exhibited a D-Q delay (DQD) of 15.7/15.47/13.51/6.611 pS, 15.33/12.18/10.48/9.239 pS, and 37.13/26.1/21.04/23.45 pS, respectively, at a V_{DD} of 0.7/0.8/0.9/1.0 V at 27 °C. The RTFF, REFF and SSPL have shown a power consumption of 4.194/9.702/12.24/22.16 µ W,4.281/6.853/11.17/17.47 µW, and 3.389/6.125/8.513/21.54 µW, respectively, at a V_{DD} of 0.7/0.8/0.9/1.0 V at 107 °C. On the other hand, RTFF, REFF and SSPL exhibited a DQD of 22.67/21.6/19.53/9.537 pS, 21.53/16.69/13.99/12.23 pS, and 56.2/35.24/27.8/23.45 pS, respectively, at a V_{DD} of 0.7/0.8/0.9/1.0 V at 107 °C. These D-FFs are considered as most promising for future self-powered or battery-operated internet of things devices and portable devices such as tablets, mobiles, laptops, smart phones,and similar handheld devices.

Keywords

CMOS, Flip-flops, Internet of things, Ultra-low power, V_{DD} scaling

Introduction

NTV (Near-threshold voltage) computing has gained tremendous attention in recent years for better energy efficiency, but it's V_{DD} down scaling is restricted by the failures in functionality induced by increased variation [1]. FFs are the fundamental sequential logic components in majority of synchronous digital integrated circuits (ICs), have a huge impact on the total power consumption, size, robustness, and performance of digital systems [2, 3]. Minimum chip area, minimized dynamic power consumption,zero redundant clock signal transitions, contention free signal transitions at NTV to eliminate failures in functionality and completely static operation to eliminate leakages at NTV are the key characteristics required for the sequential logic ICs operating at NTV [4]. FFs are the main elements in digital systems and ICs, and these FFs dominate the total power andchip area of digital systems and circuits. FFs usually consumehigh amount of dynamic power in system on chips because of their redundant and clock translations even there isno change in input data [5-8].

With the growing demand for energy-constrained portable devices such as tablets, mobiles, laptops, smart phones and similar handheld devices, low-power

IC design has increased in significance. Reduced supply voltage (V_{DD}) is one effective method of lowering circuit power consumption [9-12]. However, when V_{DD} is reduced, the sequencing elements, such as FFs, become bottlenecked because the increased variation effects severely degrade the speed and reliability of the sequencing elements.

A major issue confronting developing nanoscale computing technologies is reliability. In comparison to current CMOS technology, the majority of nanoscale electronic devices function at very low signal-to-noise ratios, leading to a high rate of transient mistakes [13]. Nanoscale CMOS technologies present substantial design issues for ICs, and variability plays a significant part in these technologies [14]. To develop an outstanding analog and physical circuit design as CMOS technologies are scaled down into the nanoscale region, a number of significant nonidealities must be addressed and overcome [15]. Random dopant fluctuations [16] in nanoscale CMOS circuits significantly alter the threshold voltage (Vt) of transistors. The operation of nanoscale circuits has been extensively investigated as nanotechnology quickly transitions from exploratory to industrial use. Therefore, in this SPICE simulation study, we studied the speed and reliability of RTFF, REFF and SSPL D-FFs at wide temperature of operations. Moreover, the V_{DD} downscaling effects on the speed and reliability of RTFF, REFF and SSPL D-FFs at wide temperature of operations also analyzed in detail.

Experimentation

RTFFs

The RTFF (Figure 1) with input-aware pre-charge technique was reported in 2021 by You et al. [6]. The input-aware pre-charge technique enables the RTFF to pre-charge the nodes only when it is essential. The RTFF is a TSPC flip-flop. Any needless internal nodes transitions ought to be eliminated in order to efficiently reduce the consumption of power by RTFF. The operation of RTFF is reported in detail [6]. The transparent mode (when CLOCK = 1) and hold mode (when CLOCK = 0) operations of RTFF with D = 0 and D = 1 inputs areillustrated in figure 2 and figure 3, respectively. Figure 4 and figure 5 indicate that the operating temperature significantly affects the short circuit power (P_{SC}) and CLOCK-to-Q_delay (CQD) and DQD of RTFF. The RTFF designed with 16 nm technology and 0.7/0.8/0.9/1.0 V V_{DD} showcased a CQD

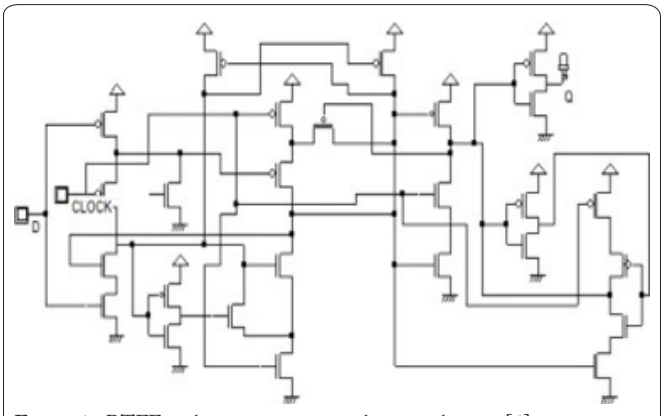

Figure 1: RTFF with input-aware pre-charge technique [6].

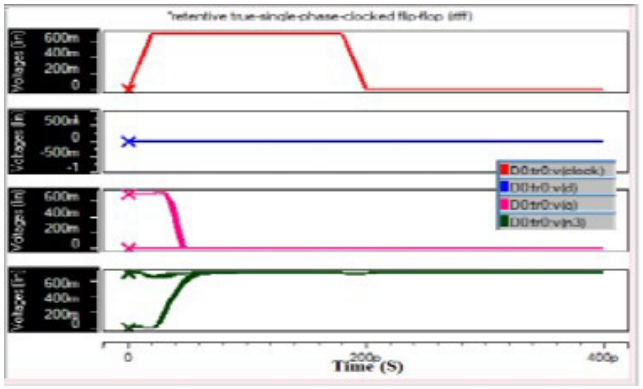

Figure 2: Transparent and hold windows of RTFF with D = 0.

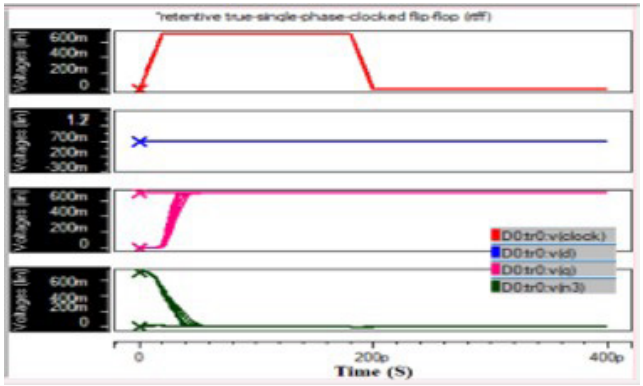

Figure 3: Transparent and hold windows of RTFF with D = 1.

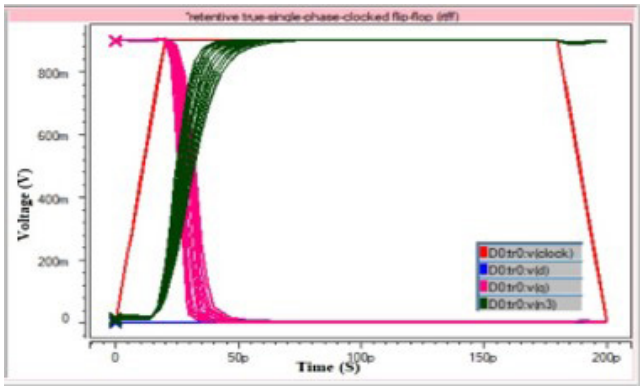

Figure 4: Operating temperature effects on RTFF with V_{DD} = 0.9 V.

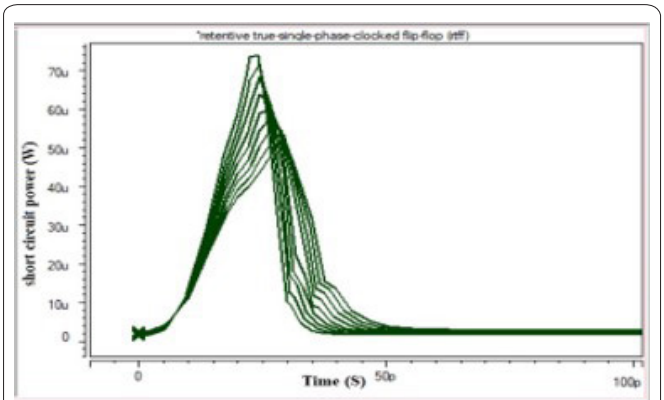

Figure 5: Operating temperature effects on P_{SC} of RTFF with V_{DD} = 0.9 V.

and power consumption of 15.7/15.47/13.51/6.611 pS and 4.803/11.67/15.97/24.34 µW and 22.67/21.6/19.53/9.537 pS and 4.194/9.702/14.24/22.16 µW at 27 °C and 107 °C, respectively (Figure 6). The rise in operating temperature significantly reduces the power consumption which leads to the increase ofCQD of RTFF.

REFF

REFF (Figure 7) was reported in 2021 by Shin et al.[1]. REFF allows V_{DD} down scaling up to 1 - 0.3 V. Redundant transistors and redundant clock signal internal transitions are eliminated in REFF to achieve ultra-low power operation. The detailed working of REFF is reported [1]. Here, we studied the speed and reliability of REFF at V_{DD} ranges from 0.7 - 1 V and operating temperature ranges from 27 °C - 107 °C. REFF is not a TSPC circuit. It uses two out of phase clock signals namely CLOCK and CLOCKB. REFF offers fully static and contention free circuit operation at ultra-low power. The transparent mode (when CLOCK = 1) and hold mode (when CLOCK = 0) operations of REFF with D = 0 and D = 1 inputs are illustrated in figure 8 and figure 9, respectively. Figure 10 and figure 11 indicate that the operating temperature significantly affects the P_{SC} and CQD and DQD of REFF. The REFF designed with 16 nm technology and 0.7/0.8/0.9/1.0 V V_{DD} demonstrated a CQD and power consumption of 15.33/12.18/10.48/9.239 pS and 4.996/8.671/12.95/19.9 µW, and 21.53/16.69/13.99/12.23 pS and 4.281/6.853/11.17/17.47 µW at 27 °C and 107 °C, respectively (Figure 12). The rise in operating temperature significantly reduces the power consumption which leads to the increase ofCQD of REFF also. The down scaling of V_{DD} from

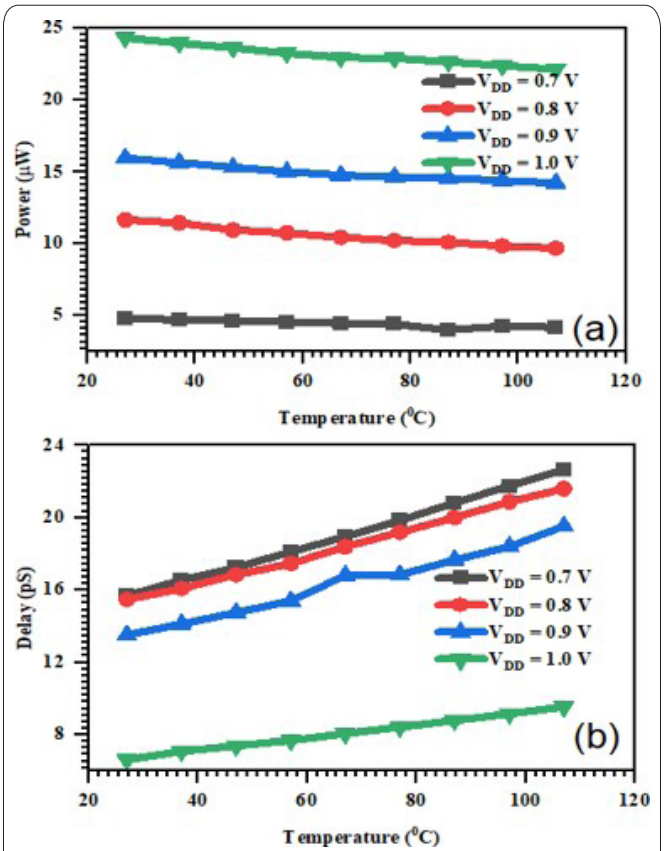

Figure 6: V_{DD} scaling and temperature effects on RTFF.

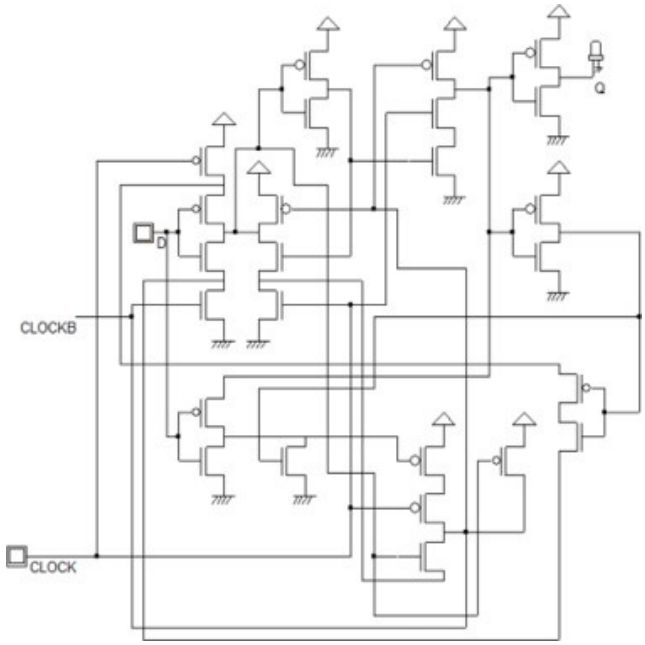

Figure 7: REFF schematic diagram [1].

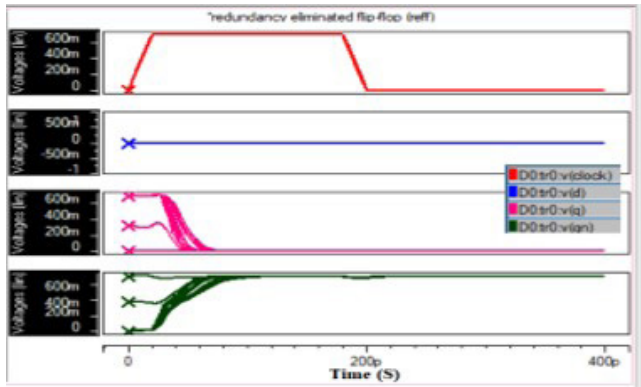

Figure 8: Transparent and hold windows of REFF with D = 0.

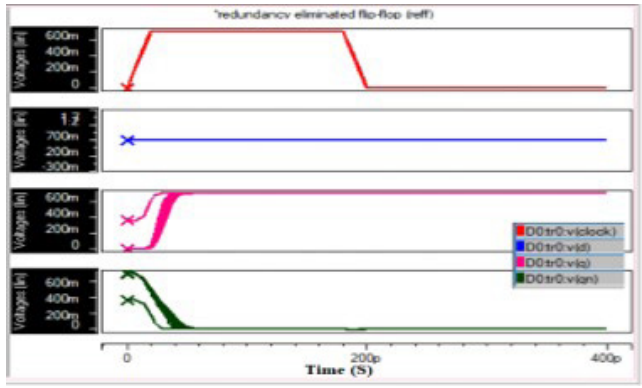

Figure 9: Transparent and hold windows of REFF with D = 1.

1 V to 0.7 V leads to 74.90% and 75.5% reduction in power consumption of REFF at 27 °C and 107 °C, respectively. On the other hand,down scaling of V_{DD} from 1 V to 0.7 V leads to 39.74% and 43.20% increase in CQD of REFF at 27 °C and 107 °C, respectively.

REFF showcased a P_{SC} of 66 µW at 107 °C and 34 µW at 27 °C. That is, P_{SC} of REFF increased by 48.49% for a rise in

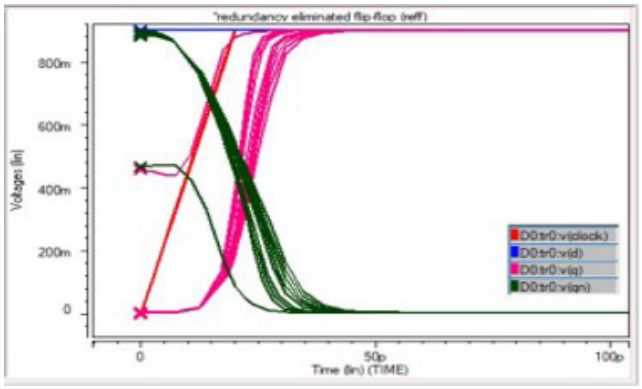

Figure 10: Operating temperature effects on REFF with V_{DD} = 0.9 V.

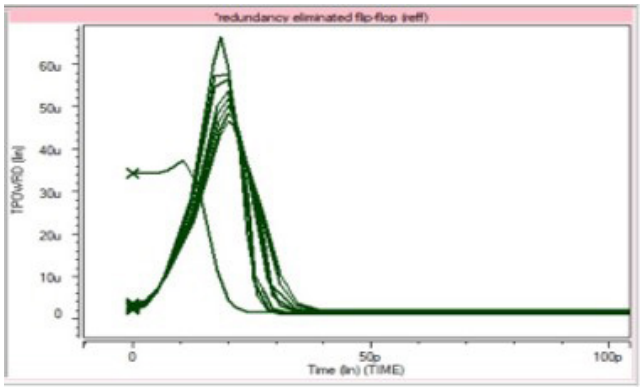

Figure 11: Operating temperature effects on P_{SC} of REFF with V_{DD} = 0.9 V.

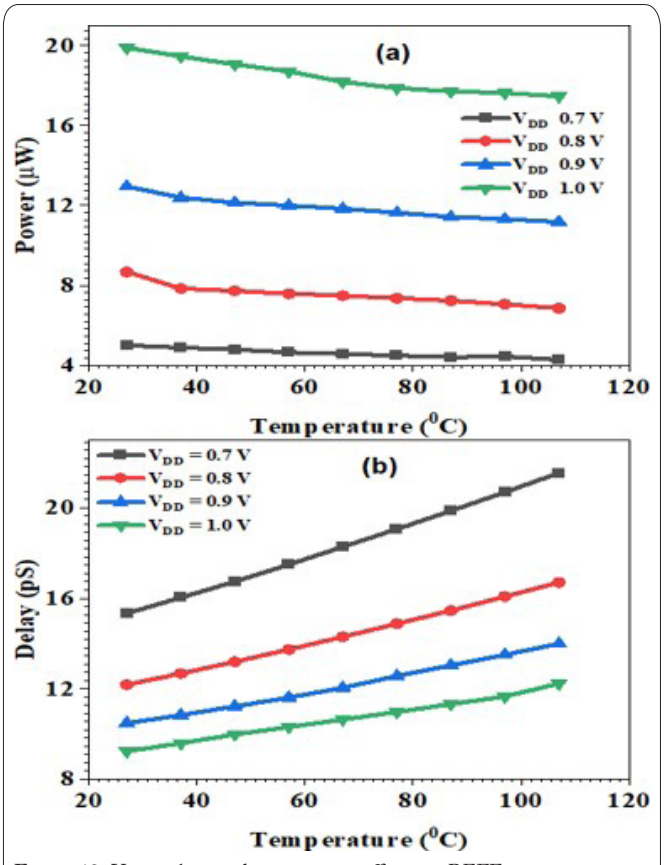

Figure 12: V_{DD} scaling and temperature effects on REFF.

operating temperature from 27 ˚C to 107 ˚C. Moreover, REFF experienced a 14.32% reduction in power consumption and 28.80% increase in CQD for a rise in operating temperature from 27 ˚Cto 107 ˚C.

SSPL

SSPL (Figure 13) was reported in 2022 by Park and Jeong [17]. SSPL is found to be effective in minimizing hold time constraint. In SSPL, the transparent window will be closed soon after the successful capturing ofthe input data. Hence, the name self-shut-off. The detailed working of SSPL is reported [17]. Here, we intensively investigated the speed and reliability of SSPL at V_{DD} ranges from 0.7 - 1 V and operating temperature ranges from 27 ˚C - 107 ˚C. SSPL is also not a TSPC circuit. It also uses two out of phase clock signals namely CLOCK and CLOCKB like REFF. The transparent mode (when CLOCK = 1) and hold mode (when CLOCK = 0) operations of SSPL with D = 0 and D = 1 inputs are illustrated in figure 14 and figure15, and figure 16 and figure 17 also indicate that the operating temperature significantly affects the P_{SC} and CQD and DQD of SSPL like other FFs. The SSPL designed with 16 nm technology and 0.7/0.8/0.9/1.0 V V_{DD} demonstrated a CQD and power consumption of 37.13/26.1/21.04/17.64 pS and 3.746/7.762/14.62/26.22 µW, and 56.2/35.24/27.8/23.45 pS and 3.389/6.125/8.513/21.54 µWat 27 ˚C and 107 ˚C, respectively (Figure 17). Like RTFF and REFF, the rise in operating temperature significantly reduces the power consumption which leads to the increase of CQD of SSPL also. The down scaling of V_{DD} from 1 V

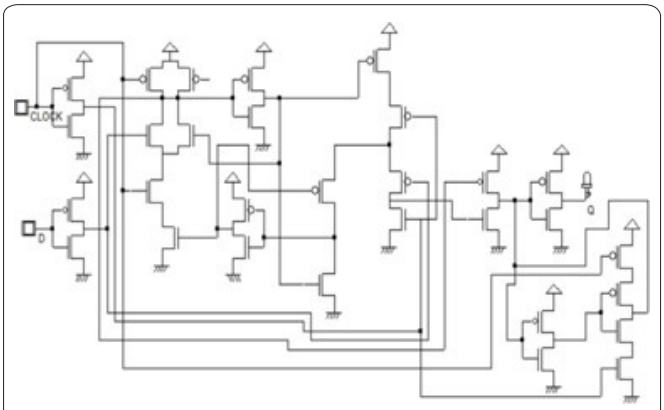

Figure 13: SSPL schematic diagram [10].

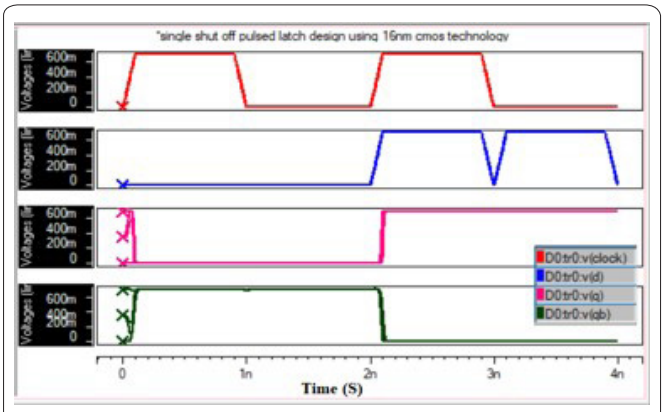

Figure 14: Transparent and hold windows of SSPL with D = 0 and D = 1.

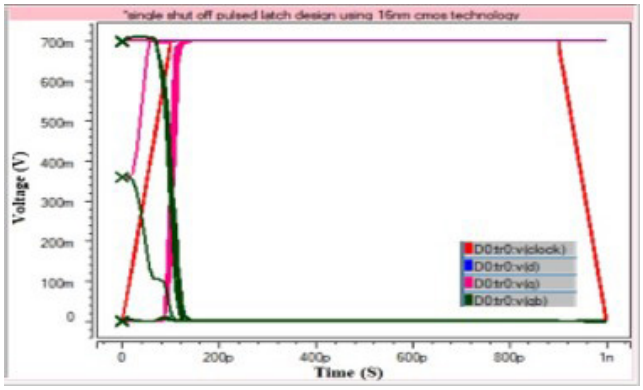

Figure 15: Transparent window of SSPL with D = 0 and V_{DD} = 0.7 V.

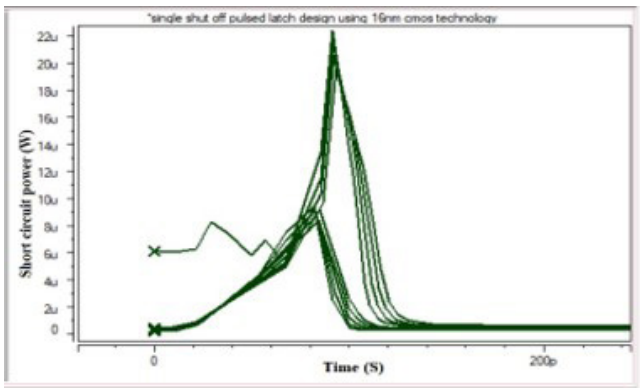

Figure 16: Operating temperature effects on P_{SC} of SSPL with V_{DD} = 0.7 V.

to 0.7 V leads to 85.71% and 84.27% reduction in power consumption of SSPL at 27 °C and 107 °C, respectively. On the other hand, downscaling of V_{DD} from 1 V to 0.7 V leads to 52.49% and 48.27% increase in CQD of SSPL at 27 °C and 107 °C, respectively.SSPL demonstrated a P_{SC} of 22 µW at 107 °C and 8 µW at 27 °C. That is, P_{SC} of SSPL increased by 63.64% for a rise in operating temperature from 27 °C to 107 °C. Moreover, SSPL experienced a 9.53% reduction in power consumption and 33.93% increase in CQD for a rise in operating temperature from 27 °C to 107 °C.

Conclusion

Here, we report the speed and reliability performance comparison of RTFF, REFF and SSPL FFs designed with 16 nm CMOS process and a V_{DD} of 0.7 - 1 V using SPICE simulations carried out at a temperature of 27 °C to 107 °C. In RTFF, REFF and SSPL, the rise in operating temperature significantly reduces the power consumption which leads to the increase of CQD ofSSPL. Down scaling of V_{DD} from 1 V to 0.7 V leads to reduction in power consumption of RTFF, REFF and SSPL at 27 °C and 107 °C. On the other hand, down scaling of V_{DD} from1 V to 0.7 V leads to increase in CQD of RTFF, REFF and SSPLat 27 °C and 107 °C. The P_{SC} of RTFF, REFF and SSPL increased with the rise in operating temperature from 27 °C to 107 °C. Moreover, RTFF, REFF and SSPL experienced a reduction in power consumption and increase in CQD for a rise in operating temperature from 27 °C to 107 °C.

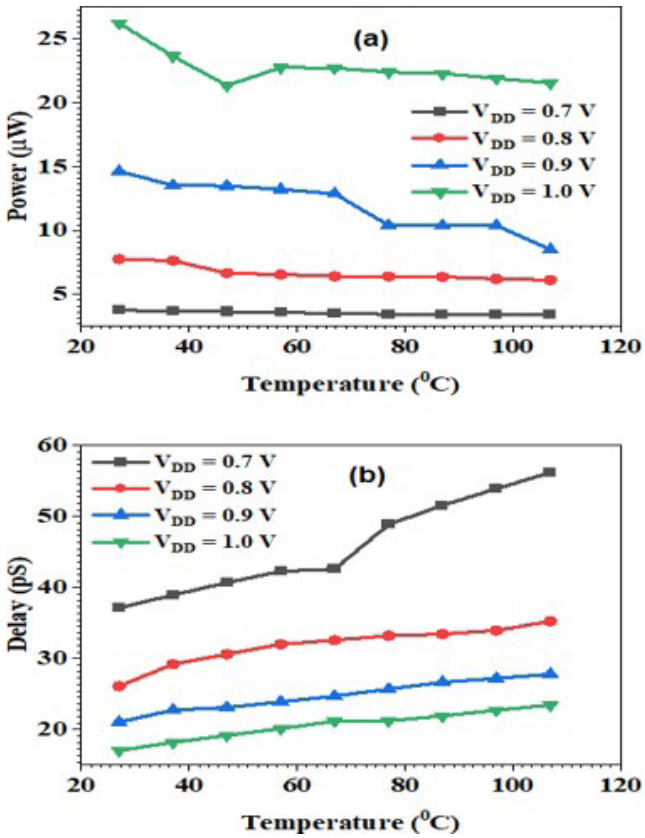

Figure 17: V_{DD} scaling and temperature effects on SSPL.

Acknowledgements

None.

Conflict of Interest

None.

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