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Research Article

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Innovative Designs of Binary-to-gray Code and Gray-to-binary Code Converters Based on QCA Nanotechnology

Sankit Kassa[1], Srujana Nandoju[2], Narendra Vadthiya[2] and Vijay Lamba[1*]

[1]Department of Electronics and Telecommunication Engineering, Symbiosis Institute of Technology, Symbiosis International Deemed University, Pune, Maharashtra, India

[2]Department of Electronics and Communication Engineering, National Institute of Technology, Warangal, Telangana, India

***Correspondence to:**
Vijay Lamba
Department of Electronics and Telecommunication Engineering,
Symbiosis Institute of Technology,
Symbiosis International Deemed University,
Pune, Maharashtra, India.

E-mail: vijay.lamba@sitpune.edu.in

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Abstract

The performance of CMOS technology-based circuits has been affected because of channel length scaling, which had an impact on increased leakage current and more power dissipation in the overall circuit. QCA (Quantum-dot cellular automata) technology has the potential to overcome these challenges as it has an edge over higher operating frequency (THz), low power dissipation (nW), and less area. The proposed work shows an efficient implementation of an XOR gate (~60% in terms of area), 3-bit and 4-bit binary to gray, and 3-bit and 4-bit gray to binary code converters with a minimum number of QCA cells and latency than already prevailing designs. This paper shows various layout design implementations which have been designed using QCA designer tool version 2.0.3.

Keywords

Quantum-dot cellular automata, QCA designer tool, Code converter

Introduction

While the size of MOSFET has become smaller, chips based on it has good performance like higher speed and reduced power dissipation. This has led to its usage in a variety of applications. But beyond 10 nm, because of short channel effects and increased power dissipation the usage of CMOS based chips is becoming limited. In order to overcome all these problems, several researchers were curious to find the solution which could be a best substitute for CMOS technology. This led to research on new nanotechnology called QCA. It is considered to be an alternative technology as it provides very high frequency in terms of THz and low power dissipation (nW) due to almost zero leakage current, unlike CMOS technology [1-6]. A QCA cell is the fundamental building block. Unlike CMOS technology, here transfer of charge happens through the columbic interaction between the electrons present in the cell. XOR gate has lot of applications such as in code converters, error correction or detection which are most commonly used in computers, digital electronics, and microprocessors.

QCA fundamentals

QCA is considered to be an emerging technology that gives another approach to nano-level computation.

QCA basics

The standard QCA cell comprises of 4 quantum dots which are occupied by only 2 electrons. A quantum dot is typically of size around (2 - 10 nm) that is capable of trapping electrons in three dimensions [7, 8]. They are the places

where a charge can be localized. Due to the repulsion of two electrons inside the cell, they both occupy diagonally opposite places. As shown in figure 1a, because of the high potential barrier the electron cannot tunnel from one QCA cell to another adjacent cell [9].

Because of the repulsion between two electrons, they occupy either of one of the above two possible diagonal positions. As shown in figure 1b, each position corresponds to a different polarization. Right diagonally aligned or polarization +1 corresponds to logic state 1. Similarly left diagonally aligned or polarization -1 corresponds to logic state 0.

Majority gate

3-input majority gate (Figure 2) is the fundamental building block in designing QCA based circuits. The center cell or device cell as shown will interact with three inputs and produces an output which is majority of all the three inputs [10-14]. The logical expression of the same is shown below.

$$Y(o/p) = A.B + B.C + C.A$$

It is the basic building block for designing logic gates like AND, OR, XOR, etc.

Related work

Code converters are combinational circuits that convert one code to its equivalent other code. These are mainly used to improve the efficiency of signal processing systems where two systems use different codes for same data to be transmitted.

In this work, an exclusive OR gate is designed, and it is used in designing efficient 3-bit and 4-bit binary-to-gray, and grey-to-binary code converters with fewer QCA cells and latency. QCA layout, simulation, and comparison results for all the designs is presented in the paperwork.

Experimentation

Design of XOR gate

XOR gates are the foundation gates of many arithmetic circuits. They are used in error-detection, correction circuits and in code converters. The logical operation of exclusive-OR (XOR) gate is shown below (Figure 3).

$$Y = A \oplus B = A'B + AB'$$

The QCA layout of efficient XOR gate is shown in figure 4. This XOR gate design consists of only 12 QCA cells, 0.016 μm^2 area and produces the output in 2 clock cycles with a latency of 0.5. This design has 67 % lesser number of cells with a similar latency than existing designs [15].

The output simulation waveforms shown above matches exactly with the logical expression of XOR gate.

Design of binary-to-gray (B-to-G) code converters

XOR gate is the fundamental unit for designing code converter circuits. The XOR gate shown in figure 4 is used for implementing efficient designs of code converters. Figure 5 presents the output waveform of XOR gate.

Design of 3-bit B-to-G code converter

This code converter basically translates input binary bits to its corresponding gray code. The block diagram and logical expressions is shown in figure 6.

$$G_2 = B_2$$

$$G_1 = B_2 \oplus B_1$$

$$G_0 = B_1 \oplus B_0$$

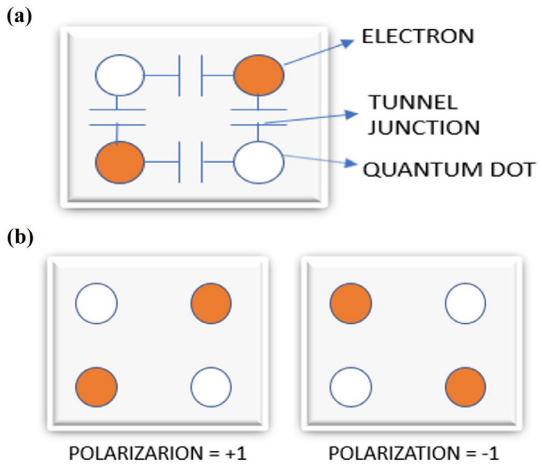

Figure 1: (a) QCA cell and **(b)** Polarity of QCA cell.

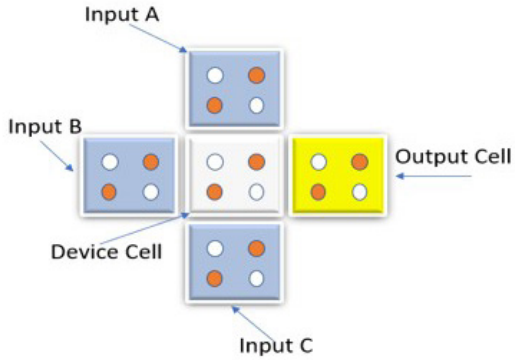

Figure 2: 3-input majority gate.

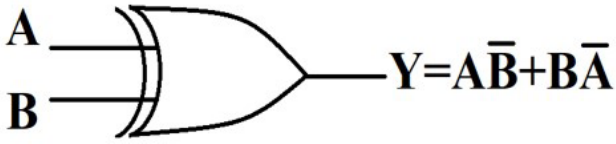

Figure 3: Block diagram of XOR gate.

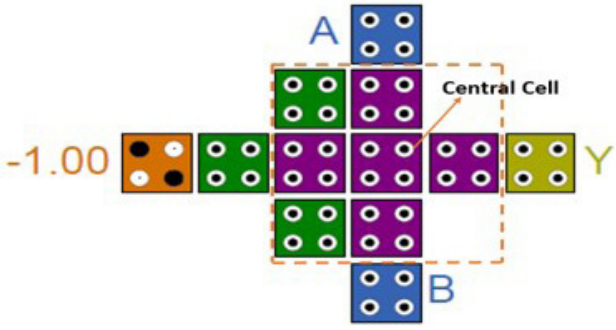

Figure 4: QCA layout of XOR gate.

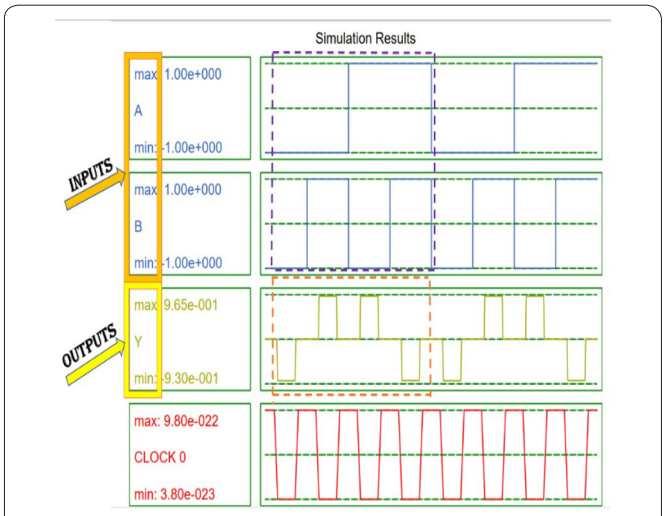

Figure 5: Output waveform of XOR gate.

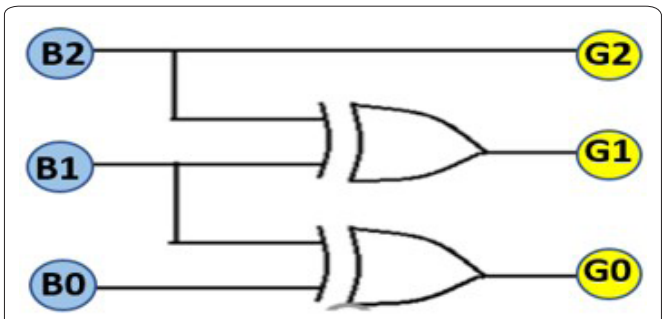

Figure 6: Block diagram of 3-bit B-to-G code converter.

Using this topology of XOR gate (figure 4) in general for n-bit B-to-G code converter designs we require only two clock cycles to produce the output. QCA layout is shown in figure 7. This implemented design has 25 QCA cells and produces the desired output within two clock cycles or with a latency of 0.5.

Design of 4-bit B-to-G code converter

Similarly for 4-bit B-to-G code converter, the block diagram (Figure 8) and logical expressions is shown below. QCA layout is shown in figure 9.

$G_3 = B_3$

$G_2 = B_3 \oplus B_2$

$G_1 = B_2 \oplus B_1$

$G_0 = B_1 \oplus B_0$

This implemented design consists of 37 QCA cells and produces the desired output within two cycles or with a latency of 0.5.

Design of gray-to-binary (G-to-B) code converters

Design of 3-bit G-to-B code converter

The block diagram (Figure 10) and logical expressions for 3-bit G-to-B code converter is shown below.

$B_2 = G_2$

$B_1 = B_2 \oplus G_1$

$B_0 = B_1 \oplus G_0$

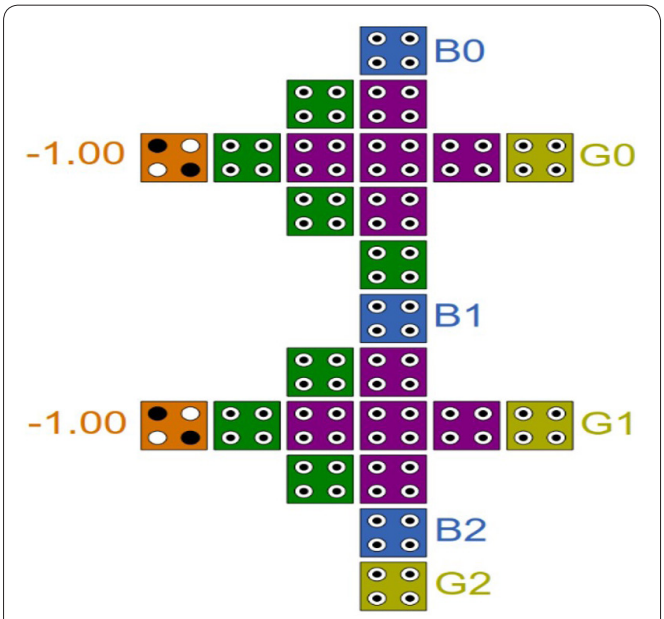

Figure 7: QCA layout of 3-bit B-to-G code converter.

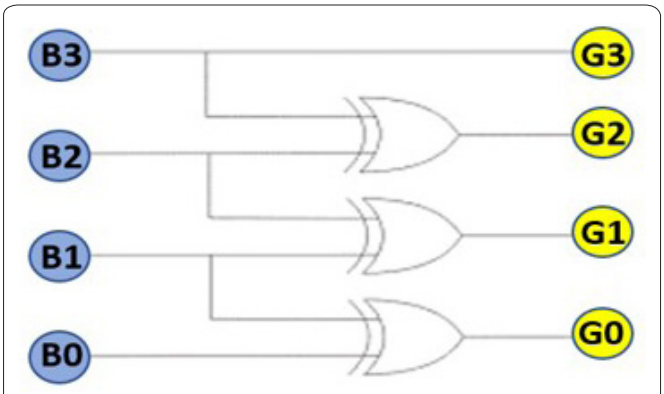

Figure 8: Block diagram of 4-bit B- to-G code converter.

Using this topology of XOR gate in general for n-bit G-to-B code converter we require n clock cycles as here there is a dependency of previous bit output. QCA layout is shown in figure 11. The implemented design consists of 26 QCA cells and produces the desired output within three clock cycles or with a latency of 0.75.

Design of 4-bit G-to-B code converter

The block diagram (Figure 12) and logical expression of 4-bit G-to-B code converter is shown below. QCA layout is shown in figure 13.

$B_3 = G_3$

$B_2 = B_3 \oplus G_2$

$B_1 = B_2 \oplus G_1$

$B_0 = B_1 \oplus G_0$

The implemented design consists of 41 QCA cells and produces the desired output within four clock cycles or with a latency of 1.

Results and Discussion

All the above designs have been implemented, simulated,

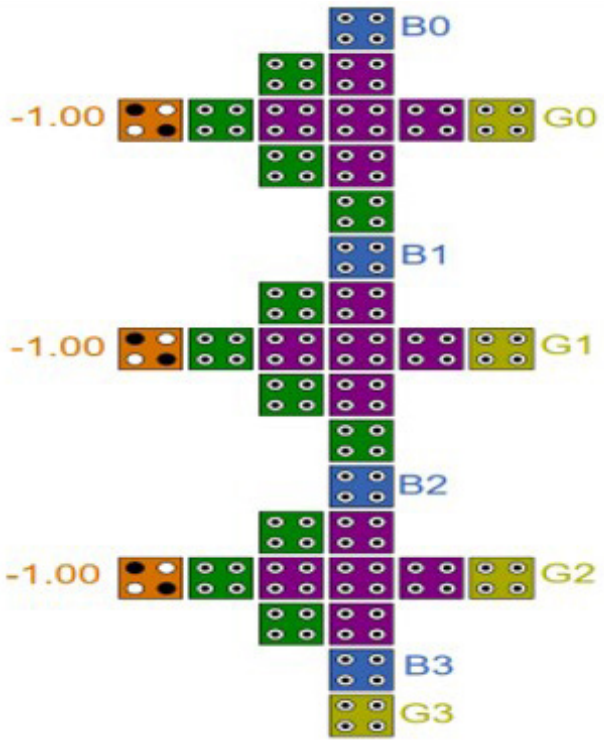

Figure 9: QCA layout of 4-bit B- to-G code converter.

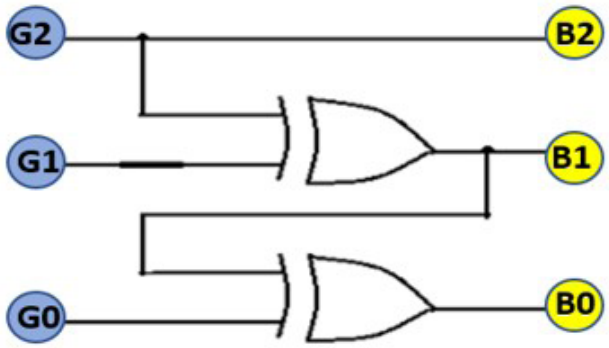

Figure 10: Block diagram of 3-bit G-to-B code converter.

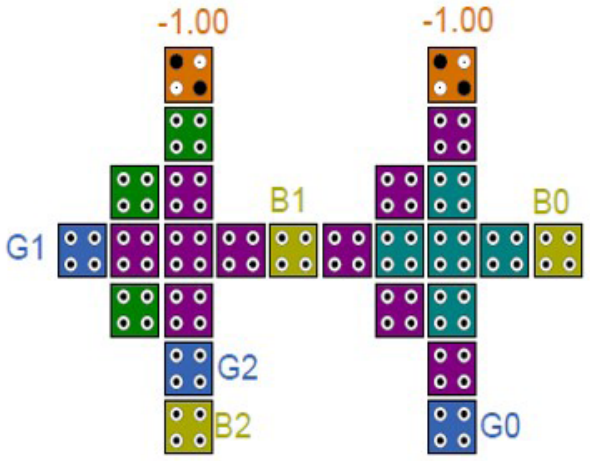

Figure 11: QCA layout of 3-bit G-to-B code converter.

and verified using QCADesigner tool. The output waveforms (Figure 14, figure 15, figure 16, and figure 17) shown in the

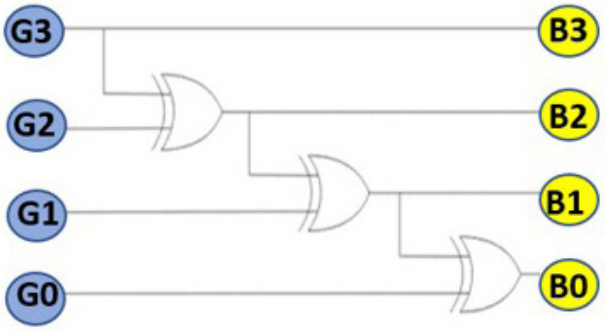

Figure 12: Block diagram of 4-bit G-to-B code converter.

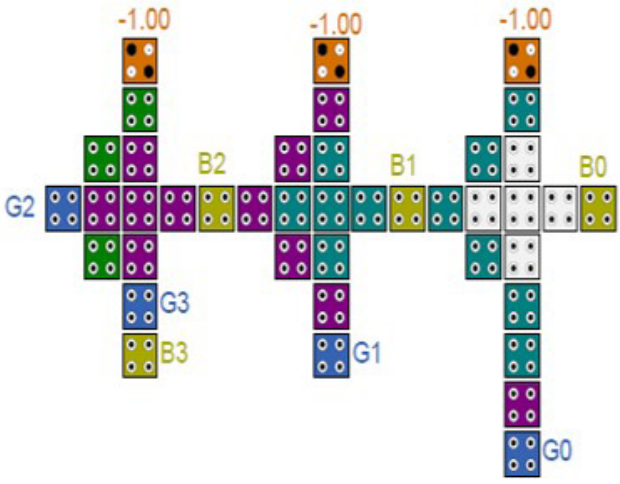

Figure 13: QCA layout of 4-bit G-to-B code converter.

Figure 14: QCA layout of 3-bit B-to-G code converter.

simulation part matches exactly with their corresponding truth table as listed which verifies the logic functionality. Additionally, comparison charts for all the above designs with respect to other reference designs is also presented (Figure 18).

Conclusion

In this manuscript, implementations of XOR gate, 3-bit

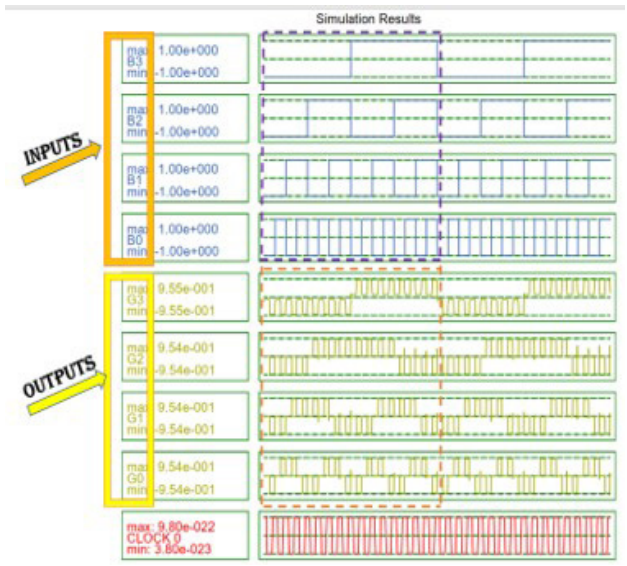

Figure 15: QCA layout of 4-bit B-to-G code converter.

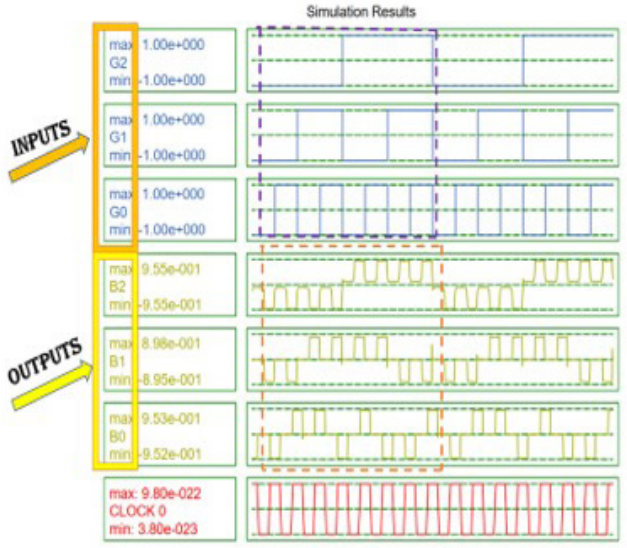

Figure 16: QCA layout of 3-bit G-to-B code converter.

and 4-bit B-to-G, and G-to-B code converters are offered with minimum latency and area. The obtained outcomes show the superiority of the proposed circuits when compared to existing advanced designs. One more advantage is that the implementations are in a single layer with zero cross-over with the wiring. Due to this advantage, it provides trouble free operation at higher temperatures. Additionally, the proposed designs also require less simulation time and device execution time. These designs also provide better performance when compared to existing CMOS technology, and hence QCA is viewed as emerging nanotechnology.

Acknowledgements

None.

Conflict of Interest

None.

Figure 17: QCA layout of 4-bit G-to-B code converter.

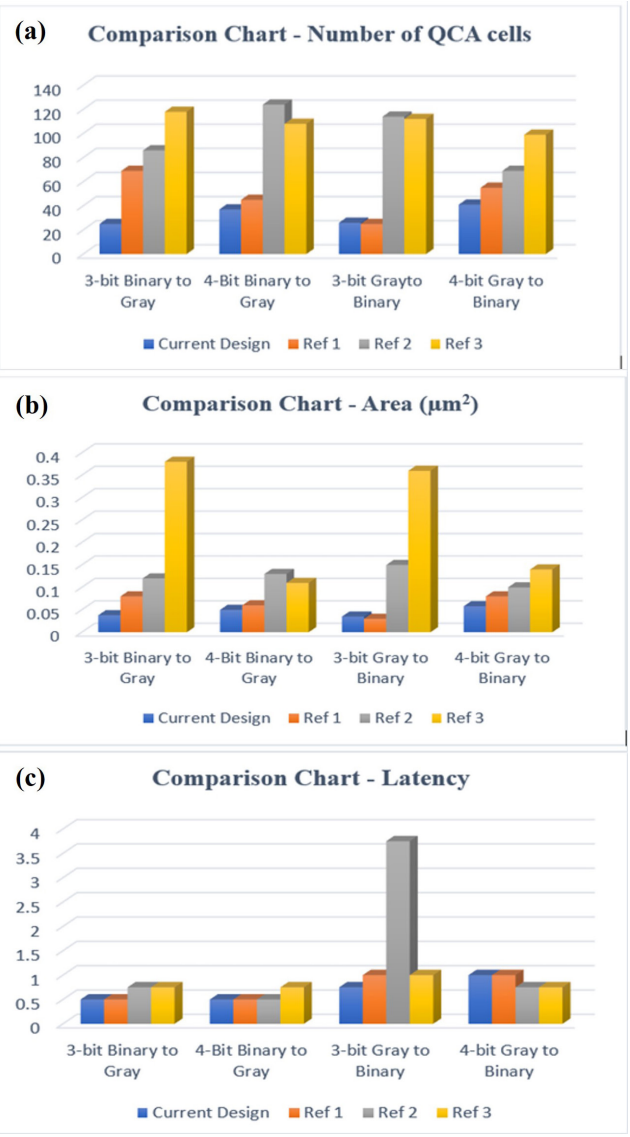

Figure 18: Comparison chart for the proposed circuit for **(a)** Number of QCA cells, **(b)** Area, and **(c)** Latency.

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