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Research Article

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A Comprehensive Study on Scalability and Thermal Reliability of Positive/Negative Edge Triggered TSPC-D Flip Flops

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Abstract

This paper studies the scalability and thermal reliability of Positive/Negative Edge Triggered type True Single Phase Clock-D Flip Flops (PET/NET-TSPC-DFFs) implemented using 16 nm, 22 nm, 32 nm and 45 nm CMOS processes with a V_{DD} (supply voltage) of 0.7 V, 0.8 V, 0.9 V and 1 V, respectively. Less transistor count and clock signal with single phase are the unique features of PET/NET-TSPC-DFFs. PET-TSPC-DFFs designed with 16 nm (V_{DD} = 0.7 V), 22 nm (V_{DD} = 0.8 V), 32 nm (V_{DD} = 0.9 V), and 45 nm (V_{DD} = 1 V) CMOS processes showcased an average power consumption of 3.019 (2.823) µW, 5.403 (4.747) µW, 10.98 (9.679) µW and 20.76 (17.89) µW at 27 °C/107 °C, respectively, and an average DQD (D-to-Q-Propagation Delay) of 12.52 (17.45) pS, 13.88 (19.38) pS, 15.54 (21.7) pS, and 16.95 (23.98) pS, respectively. On the other hand, NET-TSPC-DFFs designed with 16 nm (V_{DD} = 0.7 V), 22 nm (V_{DD} = 0.8 V), 32 nm (V_{DD} = 0.9 V), and 45 nm (V_{DD} = 1 V) CMOS processes showcased an average power consumption of 5.841 (5.016) µW, 10.66 (9.158) µW, 21.70 (18.45) µW and 41.49 (35.50) µW at 27 °C/107 °C, respectively and an average DQD of 18.55 (27.59) pS, 21.41 (31.47) pS, 23.83 (34.47) pS, and 26.09 (37.96) pS, respectively.

Keywords

CMOS process, D flip flop, Negative edge triggered, Positive edge triggered, True single phase clock

Introduction

In applications such as IoT (Internet of Things), power consumption is an important factor because IoT devices are self powered or operated by battery. Efficiently minimizing the power consumption of flip flops can significantly minimize the power consumption of digital devices and systems in IoT applications. V_{DD} scaling has been founded to be an efficient technique to diminish the power consumption of digital systems [1]. Smaller field-effect transistors (FETs) at nanoscale can enable low V_{DD} operation of flip flops [2-6]. PET/NET-TSPC-DFFs are proved to be area efficient and also offers high speed in application such as TDCs (time to digital converters), frequency dividers and data storage and PET-TSPC-DFFs are highly preferable in right shifting Vernier TDCs. On the other hand, left shifting Vernier TDCs demands NET-TSPC-DFFs [7]. Hold time (t_h), set up time (t_s), clock to Q-delay (CQD), DQD and power consumption are the key matrices used for analyzing the performance of PET/NET-TSPC-DFFs [8-19]. The utilization of electronic circuits and systems in the harsh environments like space is associated with many reliability issues including thermal and radiation effects. Since the electronic equipments used in space may not be able to replace easily once they are put into operations, their longevity (reliability) needs to be very good so that these remain perfect in their functionalities throughout the mission. Radiation and heat induced effects are the primary causes of device failures in space [17-19].

Therefore, in this work, we studied the thermal reliability and scalability of PET/NET-TSPC-DFFs by sweeping the operating temperature (T) from 27 ˚C to 107 ˚C.

Experimentation

PET-TSPC-DFFs with 16 nm CMOS process

The PET-TSPC-DFF (Figure 1) utilizes a clock signal (with only one phase) to control the hold/transparent windows. At positive edge (rising edge) of clock, M2 turns OFF and M1 turns ON if D = 1 and turns OFF if D = 0. If clock = 1 and D = 1, the nodes between M1 and M2 remains at ground potential and therefore, M5 and M6 turn OFF and the node between M5 and M6 will be charged to V_{DD} leading to turn OFF of M9 and turn ON of M7 and M8. Then nodes between M8 and M9 will be discharged to zero potential and the Q charges to V_{DD} (Figure 2 and figure 3). At rising edge of clock if D = 0, M3, M2 will turn ON and M1 will turn OFF and the node between M1 and M2 charges to V_{DD} leading the turn ON of M5 and M4 and turn OFF of M6. At this stage, node between M5 and M6 will discharge to zero potential leading the turn ON of M9 and M8 and turn OFF of M7 leading to the charging of the node between M8 and M9 to V_{DD} and therefore, the node Q discharges to zero potential (Figure 4). At the falling edge of clock, DFF will be in hold window where the Q holds the previous output value.

NET-TSPC-DFF with 16 nm CMOS process

The NET-TSPC-DFF (Figure 5) also utilizes a clock signal (with only one phase) to control the hold/transparent windows. At negative edge (falling edge) of clock, M2 turns OFF and M1 turn ON if D = 1 and turn OFF if D = 0. If clock = 0 and D = 1, the nodes between M2 and M3 remains at ground potential and therefore, M5 and M6 turn ON, M4 turns OFF and the node between M5 and M4 will be charged to V_{DD} leading to turn OFF of M9 and turn ON of M7 and M8. Then nodes between M7 and M8 will be discharged to zero potential and the Q charges to V_{DD} (Figure 6 and figure 7). At falling edge of clock if D = 0, M3, M2 will turn ON and M1 will turn OFF and the node between M2 and M3 charges to V_{DD} leading the turn OFF of M5 and M4 and turn ON of M6. At this stage, node between M5 and M4 will be discharged to zero potential leading the turn ON of M8 and M9 and turn OFF of M9 leading to the charging of the node between M8 and M7 to V_{DD} and therefore, the node Q discharges to zero potential (Figure 6 and figure 7). At rising edge of clock, DFF will be in hold window where the Q holds the previous output value.

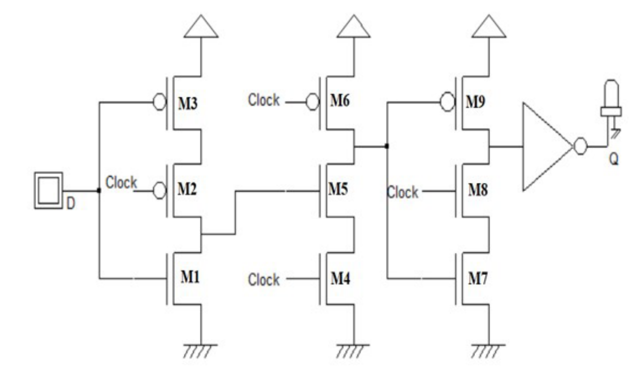

Figure 1: PET-TSPC-DFF structure [7].

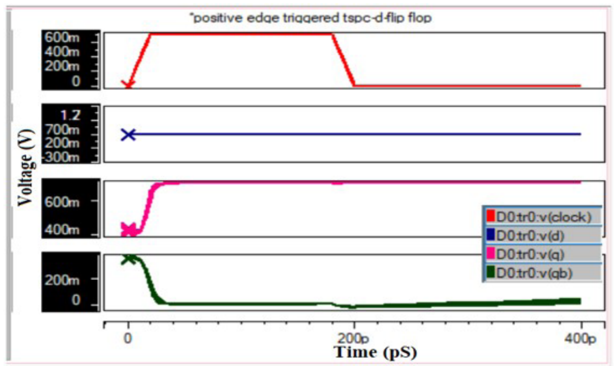

Figure 2: Transparent/hold windows of PET-TSPC-DFF with D = 1.

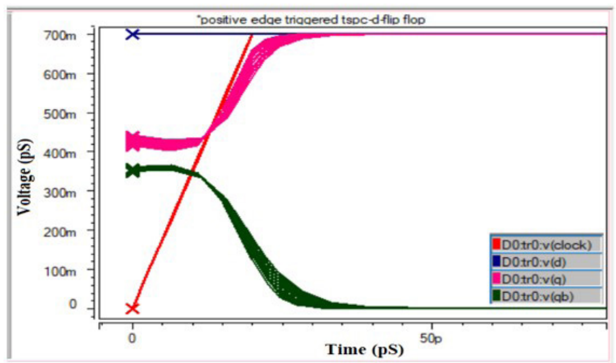

Figure 3: Transparent window of 16 nm PET-TSPC-DFF with D = 1.

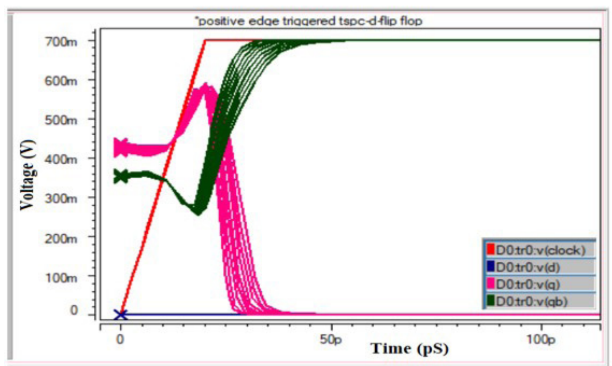

Figure 4: Transparent window of 16 nm PET-TSPC-DFF with D = 0.

Results and Discussion

Scalability of PET-TSPC-DFFs

PET-TSPC-DFFs with 16 nm CMOS process

The PET-TSPC-DFF designed with 0.7 V supply and 16 nm CMOS process showcased a power consumption and CQD of 3.019 μW (2.823 μW) and 12.52 pS (17.4 pS), respectively at 27 ˚C (107 ˚C) (Figure 8). The PET-TSPC-DFF designed

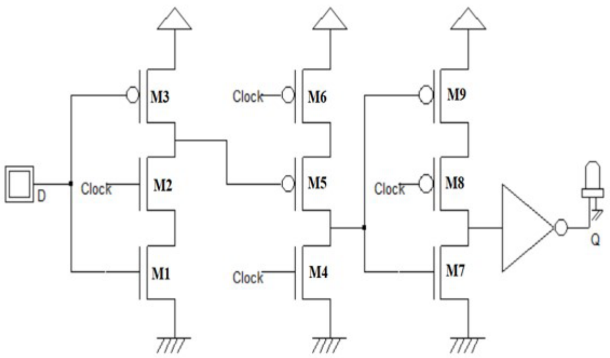

Figure 5: NET-TSPC-DFF structure [7].

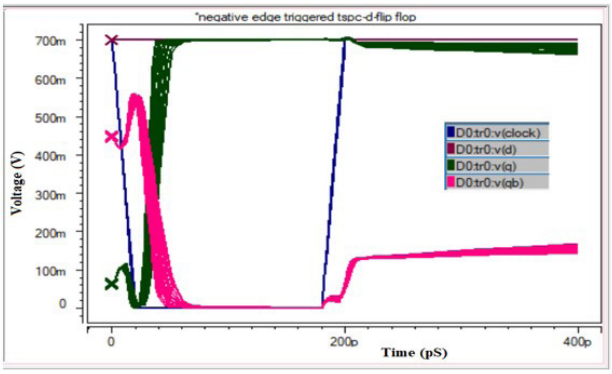

Figure 6: Transparent/hold windows of NET-TSPC-DFF with D = 1.

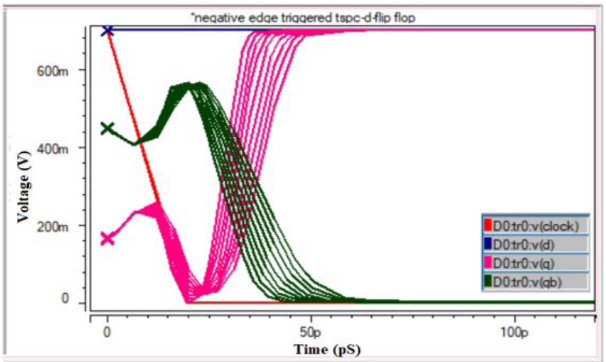

Figure 7: Transparent window of 16 nm NET-TSPC-DFF with D = 1.

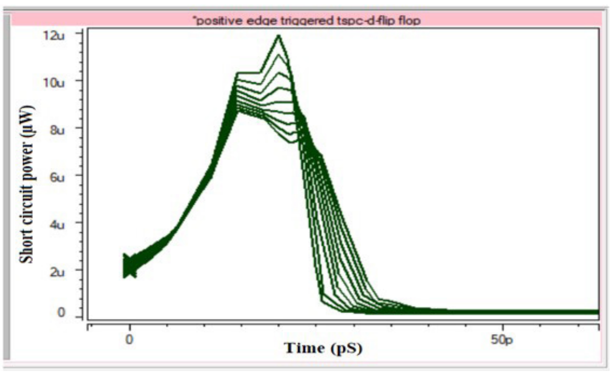

Figure 8: P_{SC} of 16 nm PET-TSPC-DFF with 0.7 V supply.

with 0.7 V supply and 16 nm CMOS process also showcased a P_{SC} (short-circuit-power) of 7.5 µW (11.9 µW) at 27 °C (107 °C). The 16 nm PET-TSPC-DFF was designed with a clock speed of 2.5 GHz and the circuit simulations were performed using SPICE tools. When T of PET-TSPC-DFF designed with 0.7 V supply and 16 nm CMOS process is elevated from 27 °C to 107 °C, power consumption is diminished by 6.5%, P_{SC} is raised by 36.98% and CQD is degraded by 28.25%. The FETs M1, M4, M5, M7 and M8 used a width of 39 nm, M2 and M3 adopted a width of 886 nm, and M6 and M9 adopted a width of 59 nm. The N and P channel FETs employed in output inverter of PET-TSPC-DFF designed with 0.7 V supply and 16 nm CMOS process are 39 nm and 118 nm, respectively.

PET-TSPC-DFFs with 22 nm CMOS process

The PET-TSPC-DFF (Figure 9 and figure 10) designed with 0.8 V supply and 22 nm CMOS process exhibited a power consumption and CQD of 5.403 µW (4.747 µW) and 13.88 pS (19.38 pS) respectively at 27 °C (107 °C). The PET-TSPC-DFF designed with 0.8 V supply and 22 nm CMOS process also showcased a P_{SC} of 13 µW (23 µW) at 27 °C (107 °C). The 22 nm PET-TSPC-DFF was also designed with a clock speed of 2.5 GHz. When T of PET-TSPC-DFF designed with 0.8 V supply and 22 nm CMOS process is elevated from 27 °C to 107 °C, power consumption is diminished by 12.14%, P_{SC} is raised by 43.48% and CQD is degraded by 28.38%. The FETs M1, M4, M5, M7 and M8 used a width of 54 nm, M2 and M3 adopted a width of 325 nm, and M6 and M9 adopted a width of 81 nm. The N and P channel FETs employed in output inverter of PET-TSPC-DFF designed with 0.8 V supply and 22 nm CMOS process are 54 nm and 162 nm, respectively.

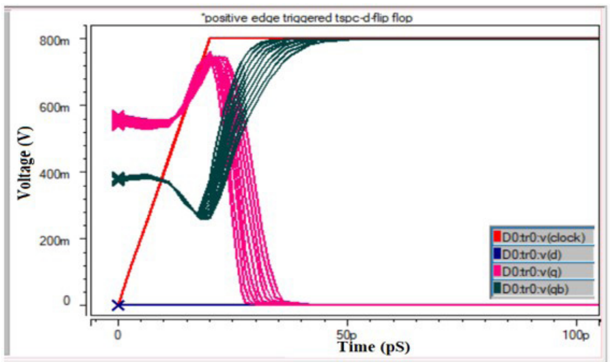

Figure 9: Transparent window of 22 nm PET-TSPC-DFF with D = 0.

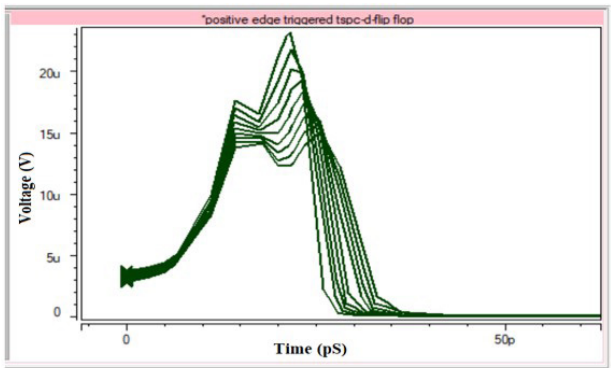

Figure 10: P_{SC} of 22 nm PET-TSPC-DFF with 0.8 V supply.

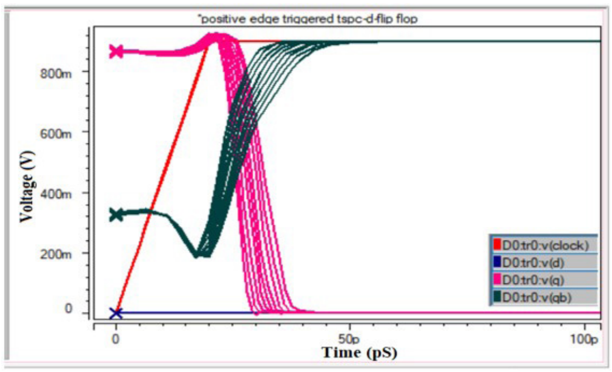

Figure 11: Transparent window of 32 nm PET-TSPC-DFF with D = 0.

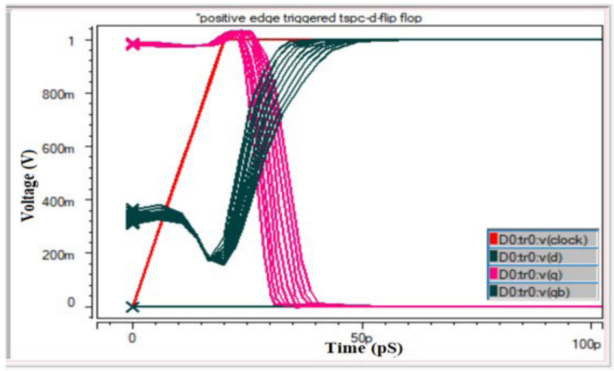

Figure 13: Transparent window of 45 nm PET-TSPC-DFF with D = 0.

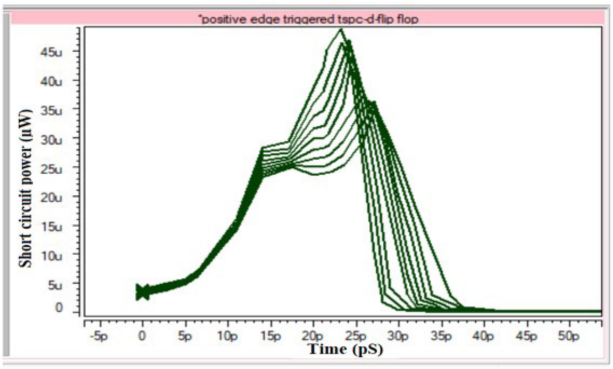

Figure 12: P_{SC} of 32 nm PET-TSPC-DFF with 0.9 V supply.

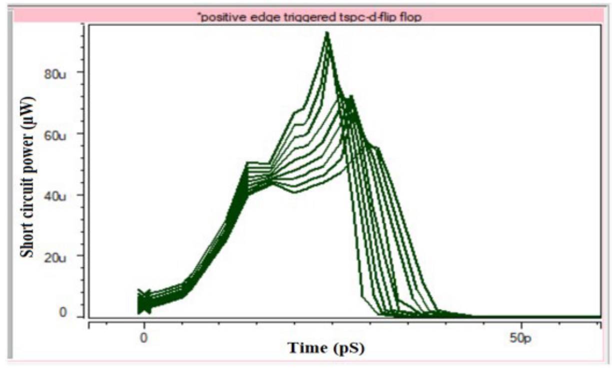

Figure 14: P_{SC} of 45 nm PET-TSPC-DFF with 1.0 V supply.

PET-TSPC-DFF with 32 nm CMOS process

The PET-TSPC-DFF (Figure 11 and figure 12) designed with 0.9 V supply and 32 nm CMOS process showcased a power consumption and CQD of 10.98 µW (9.679 µW) and 15.54 pS (21.7 pS) respectively at 27 ˚C (107 ˚C). The PET-TSPC-DFF designed with 0.9 V supply and 32 nm CMOS process also showcased a P_{SC} of 23.5 µW (49 µW) at 27 ˚C (107 ˚C). The 32 nm PET-TSPC-DFF was designed with a clock speed of 2.5 GHz. When T of PET-TSPC-DFF designed with 0.9 V supply and 32 nm CMOS process is elevated from 27 ˚C to 107 ˚C, power consumption is diminished by 11.85%, P_{SC} is raised by 52.04% and CQD is degraded by 28.39%. The FETs M1, M4, M5, M7 and M8 used a width of 79 nm, M2 and M3 adopted a width of 473 nm, and M6 and M9 adopted a width of 118 nm. The N and P channel FETs employed in output inverter of PET-TSPC-DFF designed with 0.9 V supply and 32 nm CMOS process are 79 nm and 236 nm, respectively.

PET-TSPC-DFF with 45 nm CMOS process

The PET-TSPC-DFF designed with 1.0 V supply and 45 nm CMOS process showcased a power consumption and CQD of 20.76 µW (17.89 µW) and 16.95 pS (23.98 pS), respectively at 27 ˚C (107 ˚C). The PET-TSPC-DFF (Figure 13 and figure 14) designed with 1.0 V supply and 45 nm CMOS process also showcased a P_{SC} of 56 µW (97 µW) at 27 ˚C (107 ˚C). The 45 nm PET-TSPC-DFF was also designed with a clock speed of 2.5 GHz. When T of PET-TSPC-DFF designed with 1.0 V supply and 45 nm CMOS process is elevated from 27 ˚C to 107 ˚C, power consumption is diminished by 13.82%, P_{SC} is raised by 42.27% and CQD is degraded by 29.32%. The FETs M1, M4, M5, M7 and M8 used a width of 111 nm, M2 and M3 adopted a width of 665 nm, and M6 and M9 adopted a width of 166 nm. The N and P channel FETs employed in output inverter of PET-TSPC-DFF designed with 1.0 V supply and 45 nm CMOS process are 111 nm and 332 nm, respectively (Figure 15).

Scalability of NET-TSPC-DFFs

NET-TSPC-DFF with 16 nm CMOS process

The NET-TSPC-DFF made with 0.7 V supply and 16 nm CMOS process showcased a power consumption and CQD of 5.841 µW (5.016 µW) and 18.55 pS (27.59 pS), respectively at 27 ˚C (107 ˚C). The NET-TSPC-DFF made with 0.7 V supply and 16 nm CMOS process also demonstrated a P_{SC} of 13 µW (21 µW) at 27 ˚C (107 ˚C) (Figure 16). The 16 nm NET-TSPC-DFF was designed with a clock speed of 2.5 GHz. When T of NET-TSPC-DFF designed with 0.7 V supply and 16 nm CMOS process is elevated from 27 ˚C to 107 ˚C, power consumption is diminished by 14.12%, P_{SC} is raised by 38.81% and CQD is degraded by 32.77%. The FETs M1, M2, M4 and M7 used a width of 39 nm, and M3, M5, M6, M8 and M9 adopted a width of 236 nm. The N and P channel FETs employed in output inverter of NET-TSPC-DFF designed with 0.7 V supply and 16 nm CMOS process are 39 nm and 118 nm, respectively.

NET-TSPC-DFF with 22 nm CMOS process

The NET-TSPC-DFF (Figure 17) made with 0.8 V supply and 22 nm CMOS process offered a power consumption and

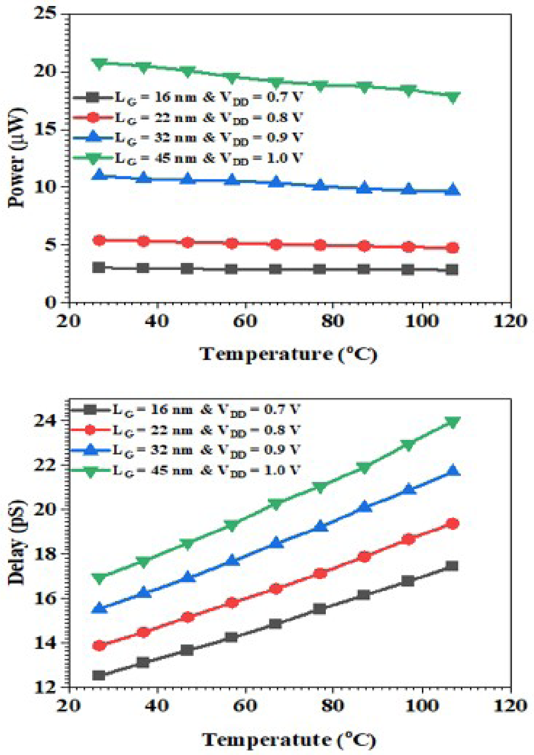

Figure 15: Thermal reliability and scalability of PET-TSPC-DFFs.

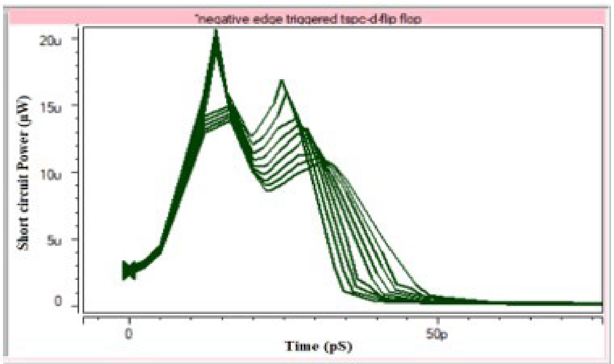

Figure 16: P_{SC} of 16 nm NET-TSPC-DFF with 0.7 V supply.

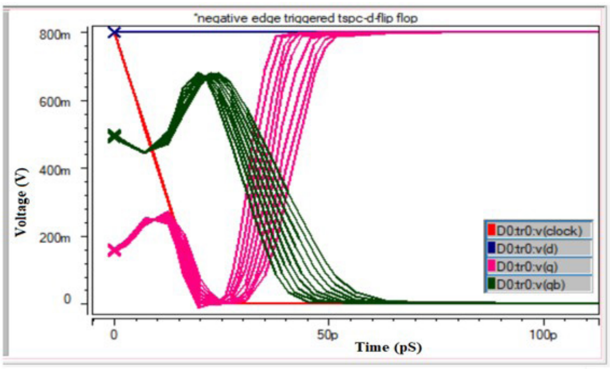

Figure 17: Transparent window of 22 nm NET-TSPC-DFF with D = 1.

CQD of 10.66 µW (9.158 µW) and 21.41 pS (31.47 pS), respectively at 27 ˚C (107 ˚C). The NET-TSPC-DFF made with 0.8 V supply and 22 nm CMOS process also demonstrated a P_{SC} of 26 µW (40 µW) at 27 ˚C (107 ˚C) (Figure 18). The 22 nm NET-TSPC-DFF was designed with a clock speed of 2.5 GHz. When T of NET-TSPC-DFF designed with 0.8 V supply and 22 nm CMOS process is elevated from 27 ˚C to 107 ˚C, power consumption is diminished by 14.10%, P_{SC} is raised by 35% and CQD is degraded by 31.97%. The FETs M1, M2, M4 and M7 used a width of 54 nm, and M3, M5, M6, M8 and M9 adopted a width of 325 nm. The N and P channel FETs employed in output inverter of NET-TSPC-DFF designed with 0.8 V supply and 22 nm CMOS process are 54 nm and 162 nm, respectively.

NET-TSPC-DFF with 32 nm CMOS process

The NET-TSPC-DFF (Figure 19) designed with 0.9 V supply and 32 nm CMOS process offered a power consumption and CQD of 21.7 µW (18.45 µW) and 23.83 pS (34.47 pS), respectively at 27 ˚C (107 ˚C). The NET-TSPC-DFF designed with 0.9 V supply and 32 nm CMOS process also exhibited a P_{SC} of 56 µW (96 µW) at 27 ˚C (107 ˚C). The 32 nm NET-TSPC-DFF was also designed with a clock speed of 2.5 GHz. When T of NET-TSPC-DFF designed with 0.9 V supply and 32 nm CMOS process is elevated from 27 ˚C to 107 ˚C, power consumption is diminished by 14.98%, P_{SC} is raised by 41.67% and CQD is degraded by 30.09%. The FETs M1, M2, M4 and M7 used a width of 79 nm, and M3, M4, M5, M7 and M8 adopted a width of 473 nm. The N and P channel FETs employed in output inverter of NET-TSPC-DFF designed with 0.9 V supply and 32 nm CMOS process are 79 nm and 236 nm, respectively (Figure 20).

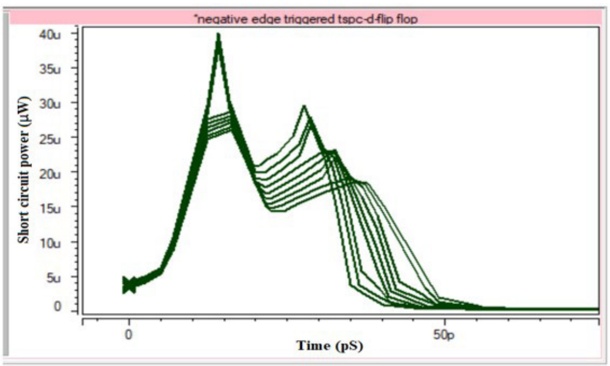

Figure 18: P_{SC} of 22 nm NET-TSPC-DFF with 0.8 V supply.

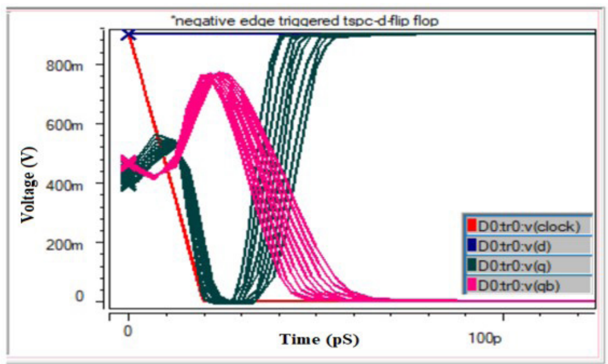

Figure 19: Transparent window of 32 nm NET-TSPC-DFF with D = 1.

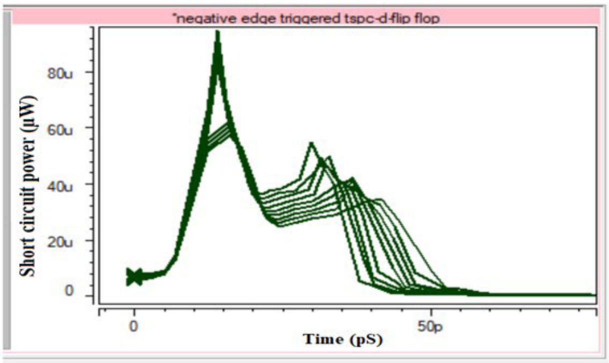

Figure 20: P_{SC} of 32 nm NET-TSPC-DFF with 0.9 V supply.

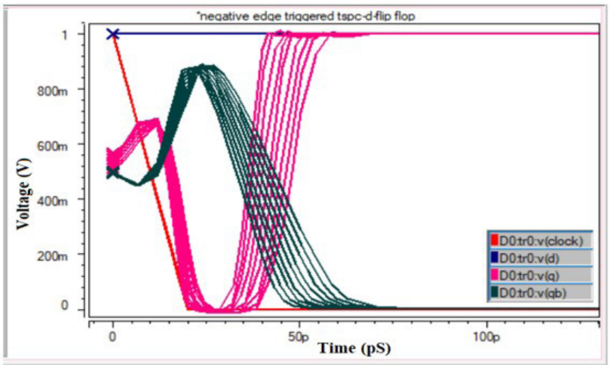

Figure 21: Transparent window of 45 nm NET-TSPC-DFF with D = 1.

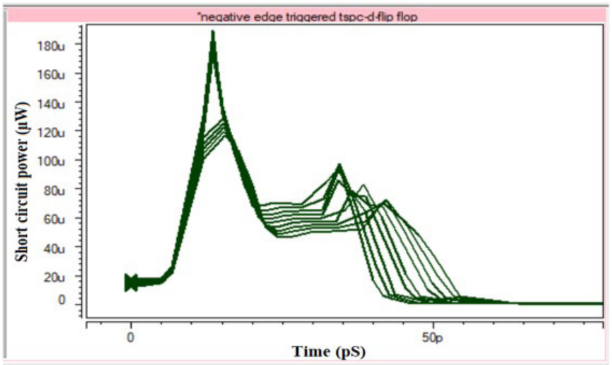

Figure 22: P_{SC} of 45 nm NET-TSPC-DFF with 1.0 V supply.

NET-TSPC-DFF with 45 nm CMOS process

The NET-TSPC-DFF (Figure 21 and figure 22) designed with 1.0 V supply and 45 nm CMOS process showcased a power consumption and CQD of 41.49 µW (35.5 µW) and 26.09 pS (37.96 pS), respectively at 27 °C (107 °C). The NET-TSPC-DFF designed with 1.0 V supply and 45 nm CMOS process also demonstrated a P_{SC} of 110 µW (186 µW) at 27 °C (107 °C). The 45 nm NET-TSPC-DFF was designed with a clock speed of 2.5 GHz. When T of NET-TSPC-DFF designed with 1.0 V supply and 45 nm CMOS process is elevated from 27 °C to 107 °C, power consumption is diminished by 14.44%, P_{SC} is raised by 40.86% and CQD is degraded by 31.27% (Figure 23). The FETs M1, M2, M3 and M7 have a width of 111 nm, and M3, M4, M5, M7 and M8 adopted a width of 665 nm. The N and P channel FETs employed in output inverter of NET-TSPC-DFF designed with 1.0 V supply and 45 nm CMOS process are 111 nm and 332 nm, respectively.

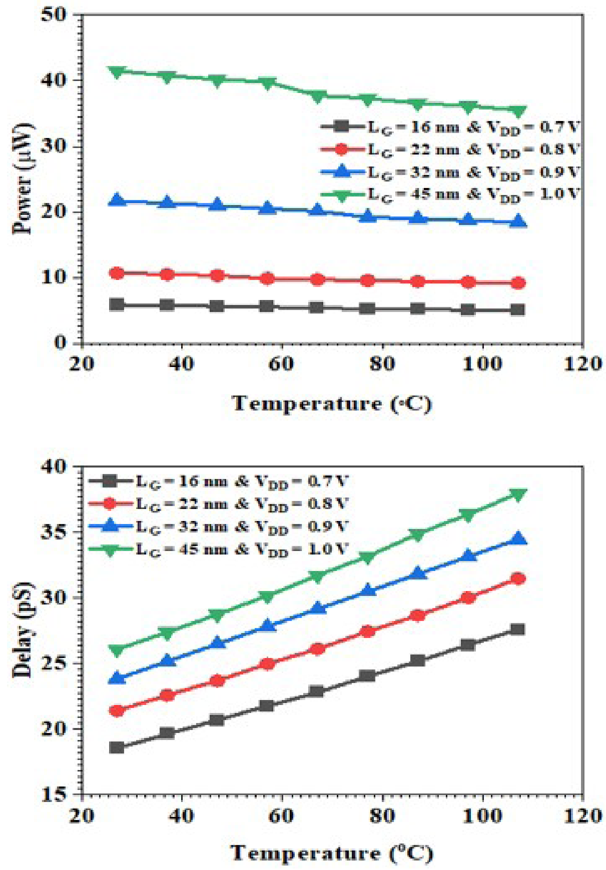

Figure 23: Thermal reliability and scalability of NET-TSPC-DFFs.

Conclusion

In this work, we report the scalability and thermal reliability of PET/NET-TSPC-DFFs. The PET/NET-TSPC-DFFs were designed and simulated using 16 nm, 22 nm, 32 nm and 45 nm CMOS processes with a V_{DD} of 0.7 V, 0.8 V, 0.9 V and 1.0 V, respectively. The power consumption of the PET (NET)-TSPC-DFFs were found to be degraded by 6.5% (14.12%), 12.14% (14.10%), 11.85% (14.98%), and 13.82% (14.44%) respectively for 16 nm (0.7 V), 22 nm (0.8 V), 32 nm (0.9 V) and 45 nm (1.0 V) CMOS processes. The CQD of the PET (NET)-TSPC-DFFs were found to be degraded by 28.25% (32.77%), 28.38% (31.97%), 28.39% (30.09%) and 29.32% (31.27%) respectively for 16 nm (0.7 V), 22 nm (0.8 V), 32 nm (0.9 V) and 45 nm (1.0 V) CMOS processes. PET/NET-TSPC-DFFs are gaining attention in the high speed and low power data storage applications.

Acknowledgements

None.

Conflict of Interest

None.

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