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Review Article

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Development of Rectangular Nanosheet GAA-FET with Underlap

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Abstract

When field effect transistors (FETs) are scaled continuously, short channel effects (SCEs) can be experienced as a result. The main objective of this paper is to analyze the GAA-FET (Gate-all-around field effect transistors) nanowire and design an underlap nanowire device and propose a nanosheet by incorporating three nanowires with underlap. Each device is stimulated, and its performance is observed. This paper investigates the effect of SCEs on the performance of nanowire GAA-FETs, with a focus on minimizing SCEs. SCEs are observed in these devices and note that some parameters are enhanced. The ON-state current is one of the factors that increase the device's performance as a result of the observed improvements. In nanosheet GAA FETs, the ON-state current is enhanced. In order to achieve a large ON-state current, designing nanowire devices with underlaps on the source and drain is one of the techniques. Three nanowires are employed to design the nanosheet GAA-FET, which consists of bulk and underlapped source/drain regions. The characteristics of all the three devices are investigated and it is seen that the ON-state current in transfer and output characteristics. By including the underlap and bulk on source/drain in the device, the ON-state current is three times higher in the nanosheet GAA-FET. The subthreshold slope varies very little. Additionally, the drain-induced barrier lowering (DIBL) of the developed device is optimized and gives the effective results.

Keywords

Underlap, Nanosheet, ON-Current, Short channel effects

Introduction

According to Moore's Law, the count of transistors on a chip doubles every 18 months, so as to increase the transistor density on the chip the transistor area is halved [1]. Continuous scaling of transistors results in limitations such as subthreshold leakage, channel length modulation, DIBL, power dissipation. A major limitation is the loss of gate control on the channel region as the channel length decreases in conventional MOSFETs the source and drain become close to each other [2]. To reduce these effects the transistors are modified into different structures. Hence, multiple gate based vertical structures are developed that plays an important role in the semiconductor industry. These structures are of different form like double gate FET, triple gate FinFET, GAA-FET, and so on [3, 4]. Nonplanar transistors are better suited for greatly scaled transistor lengths, and these devices enable superior gate-channel control. The use of multiple gates demonstrates superior electrostatic control of the channel with the possibility of a gradual reduction in channel length when compared to standard MOSFETs. This provides enhanced control of the gate in the channel region of the device. GAA device designs are of varied shapes like square, rectangular, polygon, circular. In

GAA-FETs, the gate is wrapped around the channel leading to better gate control and improvement in short channel performances.

While scaling the transistors below 14 nm gate length or so, even the GAA-FETs sublime to SCEs. But, scaling down of transistor carries on incorporating more functions in the same chip hence increasing the transistor density becomes the objective. Therefore, even with the GAA-FETs better SCEs remains the need of the hour and leakage reduction is required to increase the device performance.

Researchers came up with the technique of source/drain underlap which observed to improve the device SCEs [3]. This underlap region is introduced on either side of channel region leading to provide the additional resistance in the device also known as parasitic resistances, by this the overall resistance of the device is enhances leading to reduction in the ON current, thereby performance decreases [4]. But with the underlap, device performance can be optimized especially at nano regime, which is already under severe SCEs, as the threshold voltage decreases due to improved SCEs and corresponding gate overdrive voltage increases [3, 5]. Also, the scaling down of FETs leads to increases parasitic capacitances. In the nanoscale device, the parasitic capacitances contribute a significant portion in the overall capacitance of the device as observed in FinFETs. To reduce this parasitic capacitance introducing underlaps is perceived in literature [6]. The parasitic capacitances comprise of inner and outer fringe capacitances. In the overall capacitances, the parasitic capacitance is limited and should not exceed by 58% [7].

The increasing demands for low power consumption and high-speed system on chip application, high ON current is a critical requirement but that is not viable with induction of parasitic effects. To control the SCEs and stabilize the ON current the underlap length is required to be optimized for nanodevices [8, 9]. While scaling the thickness of the gate oxide is necessary to increase the oxide-capacitance, which increases the ON current of the device as current is directly proportional to the oxide capacitance. Hence, optimization in quite a few aspects becomes an important issue and is required to be ensued for enriched device performances.

Based on these concepts and considering the advantages of underlap, the motivation here stands as to develop a GAA-FET with the introduction of underlap of the channel extending to the source/drain region. While also the objective is to increase the ON current with optimized parasitic (resistance and capacitances) based SCEs. Hence, the focus of the paper is to develop and analyze underlap based single rectangular GAA-FET which is further reformed inducing similar device in parallel connected in series, thereby designing the nanosheet GAA-FET, adopting three nanowires with underlap without reducing the oxide thickness, to reduce the SCEs while increasing the current.

Experimentation

Device structure and simulation

Three rectangular GAA-FET devices are designed in three dimensional using SILVACO TCAD's ATLAS simulation tool The devices developed are designed at 10 nm gate length and are labelled as Device A, B, and C as tabulated in table 1, where Device A is the conventional Rectangular GAA, Device B is replica of Device A with underlap channel of 5 nm length on either side and the novel Device C having the nanosheet GAA inserted with underlaps. In both Device B and Device C the source and drain dimensions are maintained to be bigger than the channel with underlap. The 3D schematic view of a conventional rectangular GAA is shown in figure 1a. In this design of Device A, the source/drain is set to be equal to the channel. The channel is surrounded by a layer of SiO_2, and the gate metal is wrapped on top of the oxide. Using Device A as a model, Device B is developed and designed by extending the underlap on both sides of the channel to the source/drain region as shown in figure 1b. Device C is a nanosheet, which is designed by considering three nanowires placed in parallel with an underlap and the source/drain is taken as large, connecting the three nanowires shown in figure 1c. The physical device parameters listed in table 2 are used for design of devices.

SILVACO TCAD's ATLAS simulation tool is used to design and simulate all three devices. In this the device analysis, simulations are achieved by invoking physical models such as Auger recombination model, Concentration Dependent

Table 1: Device description.

Device name	Device description
Device A	Single rectangular GAA-FET
Device B	Single rectangular GAA-FET with underlap
Device C	Nanosheet GAA-FET with underlap

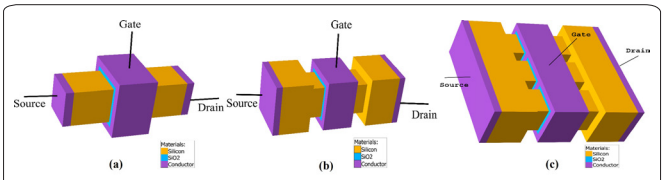

Figure 1: 3D schematic view of **(a)** single rectangular GAA-FET, **(b)** single rectangular GAA-FET with underlap, and **(c)** nanosheet GAA-FET with underlap.

Table 2: Parameters used for device design.

Parameters	Dimensions
Gate length, L_g	10 nm
Channel area	10 nm x 10 nm
Source/Drain length, $L_{S/D}$	10 nm
Underlap length, L_U	5 nm
Underlap thickness, T_U	10 nm
Source/Drain bulk length	10 nm
Oxide thickness, t_{ox}	1 nm
Metal thickness	2 nm
Oxide dielectric constant, k	3.9
Work function metal, φ_m	4.6 eV
Source/Drain doping	10^{18} cm^{-3}
Channel doping	10^{15} cm^{-3}
Mobility of electrons and holes	1400 cm^2/V-s and 450 cm^2/V-s

Mobility Model, Shockley-Read-Hall recombination method, Hansch quantum effects approximation model with Lambda of 1e-3 for N channel MOS devices, bandgap narrowing model, FERMI carriers' statics for electron and holes, and for the mathematical simulation calculations the Newton and Gummel's methods are used. The Newton and Gummel's numerical iteration are used to solve differential equation, recombination characteristics and the mobility reduction in ATLAS respectively.

Results and Discussion

All the three devices are designed using SILVACO TCAD's ATLAS device simulation tool. To analyse the device performances the two characteristic graphs are taken which represent transfer characteristics and output characteristics. The transfer characteristics I_D vs V_{GS} are determined at V_{DS} of 0.1 V and 1 V which helps in finding the threshold voltage, ON-current, transconductance, OFF-current, DIBL, I_{ON}/I_{OFF} ratio, etc. The transfer characteristics are also taken in log scale to determine the subthreshold slope. The output characteristics I_D vs V_{DS} are taken at a V_{GS} of 0.8 V.

A comparison of threshold voltages in the three devices is shown in figure 2 and it is observed that the three devices have an approximate value of the threshold voltage. Due to the scaling down of device, the channel becomes shorter as the source and drain are brought together. So, the threshold voltage also reduces as the channel length reduces and the effective channel length also reduces due to the increase in depletion region. Decreasing the effective channel length resulted in a roll-off of the threshold voltage. Device C operates at a threshold voltage of ~0.245, which is approximately equal to the value of Device A and Device B.

The transfer characteristics plotted for the three devices using linear scale shown in figure 3. From the graph, the drain current I_D is observed by varying V_{GS} (0 - 1 V). The On-state current contributes to high device performance. The transfer characteristics I_D - V_{GS} clearly illustrate that the ON-state current increases greatly in Device C, and slightly increased in Device B as compared to Device A. The increase of current in Device C is due to the use of wider transistors by connecting multiple channels together. The three nanowires are considered in designing the Device C, through which three channels are formed so the current is tripled. In Device C, the ON-state current is very high, providing a fast-switching speed and device performance. As can be seen from the transfer characteristics, a channel forms and initiates conduction in the nanosheet device with a threshold voltage of ~0.245. The maximum drain current is determined in Device C is ~338 µA/µm at V_{DS} = 1 V, which is three times higher than the drain current in Device A, which is approximately ~110 µA/µm.

In figure 4 the transfer characteristics I_D vs V_{GS} are plotted in a logarithmic scale to find the subthreshold slope of the designed devices. The Subthreshold swing determines the behavior of the FET in the subthreshold region.

It also defines the figure of merit for FET. Subthreshold swing provides a measure of how sharply a transistor can turn

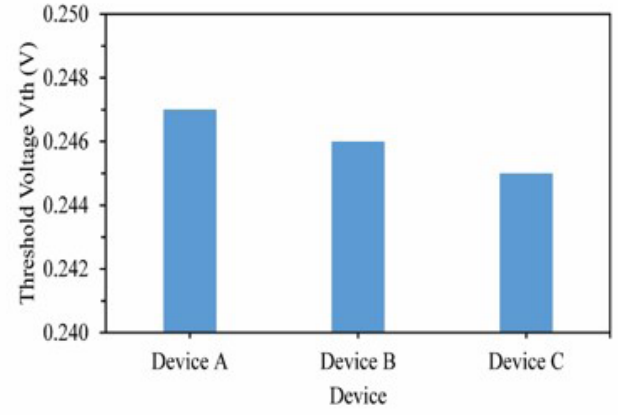

Figure 2: Comparison of threshold voltage in three devices.

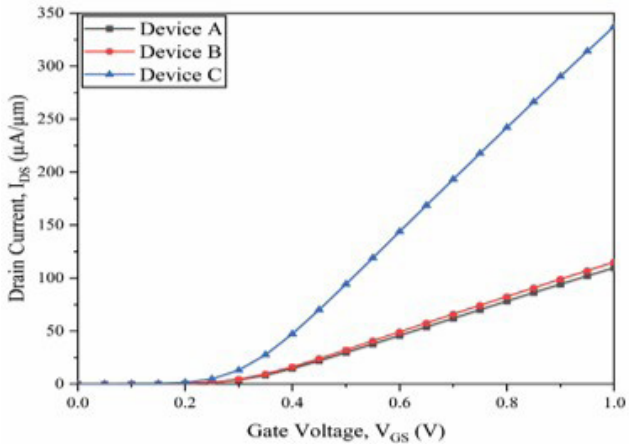

Figure 3: The transfer characteristics, I_D vs V_{GS} on linear scale at V_{DS} = 1 V.

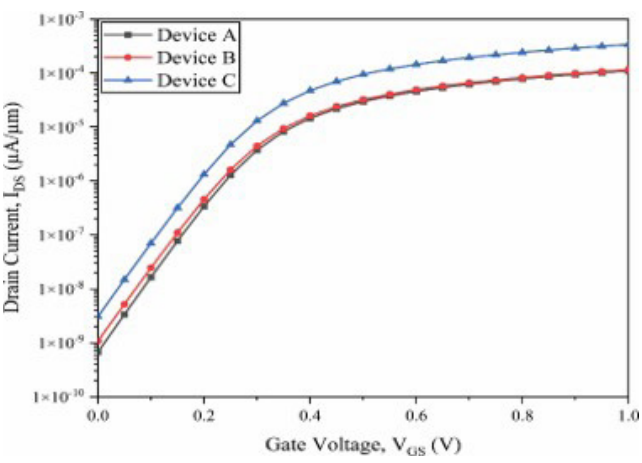

Figure 4: The transfer characteristics I_D vs V_{GS} in log scale.

ON/OFF. There appears to be a slope in the figure above and this can be observed by taking the graph on a log scale. The slope of the graph gives a subthreshold swing. Based on this graph, it is clear that the subthreshold swing is slightly increased in the proposed Device C due to the increased off state current compared to Device A and Device B. At subthreshold voltage, there is more leakage current in Device C due to the corner effect in three channels. As a result, the OFF-state current is high, the subthreshold swing is slightly increased but

the value is within an acceptable range for proposed device.

In short channel devices the current is flows below the gate voltage reaches to threshold value and this flowing of current is due minority carriers is leads to OFF current. Here the subthreshold slope is the change in gate voltage with respect to change the subthreshold drain current by one decade. A comparison of the subthreshold swing in the three devices is shown in figure 5. And it is seen that the subthreshold swing in Device A is ~71 mV/decade and Device B and Device C is ~73 mV/decade. The subthreshold voltage in Device C is better compared to Device B and it can be seen in table 3.

DIBL is another parameter in the SCEs that must be considered for shorter devices and is measure from a transfer characteristic. The ratio of the change in threshold voltages to the change in the drain voltages from low voltage to high voltage is given by DIBL. A comparison graph is shown in figure 6 and it is observed that DIBL is quite high in Device B and decreases in Device C compared to Device A, which gives the most favorable performance of the nanosheet.

The output characteristics I_D - V_{DS} is shown in the figure 7 of three devices and it is observed at V_{GS} = 0.8 V. The Device A is getting an I_D of ~84 μA/μm. Compared to Device A, the Device B is slightly increasing the drain current which is ~88 μA/μm. The Device C is getting three times higher drain current than the other devices which is equal to ~260 μA/μm. Due to using bulk source/drain along with underlap in the nanosheet the drain current in Device C increases without any change in doping concentration or mobility.

All three devices are design and stimulated in the SILVACO ALTAS TCAD tool. It is observed that parameters like threshold voltage, ON-current, DIBL are provide better results in Device C as compared to Device A and Device B and subthreshold slope is giving acceptable value. All the results are shown in table 3.

Conclusion

In the analysis of three devices, it is seen that the underlap structure is provides better performance compared to the single rectangular GAA-FETs. By observing this underlap structure advantages the nanosheet is proposed and developed by including the underlap in GAA-FETs. All three devices are designed with the channel length of 10 nm and analyzed, and it is seen that some of the SCEs gives better results. Based on the complete analysis of the three devices, it is evident that the proposed device has higher ON-state current and better values of subthreshold swing and DIBL are obtained. Subthreshold slopes are maintained near their values of ~73.06 mV/decade for all devices. DIBL is observed a value of ~58.77 mV/V in the nanosheet, which is improved compared to nanowire devices. The nanosheet GAA-FET device provides a high current of ~338 μA/μm at a threshold voltage of ~0.245 V which is more than three times of single rectangular GAA-FET. In this overall comparison of all three devices the nanosheet GAA with underlap reduces the SCEs and provides enhanced device performance being capable as a futuristic device.

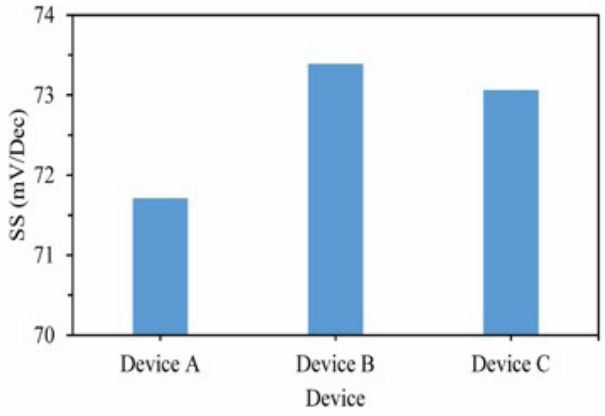

Figure 5: Comparison of subthreshold swing in three devices.

Table 3: Observed results.

Parameter/ Device	V_{th} (V)	I_{on} (μA/μm)	SS (mV/Dec)	DIBL (mV/V)
Device A	0.247	109.61	71.71	60.49
Device B	0.246	114.88	73.39	62.70
Device C	0.245	337.52	73.06	58.77

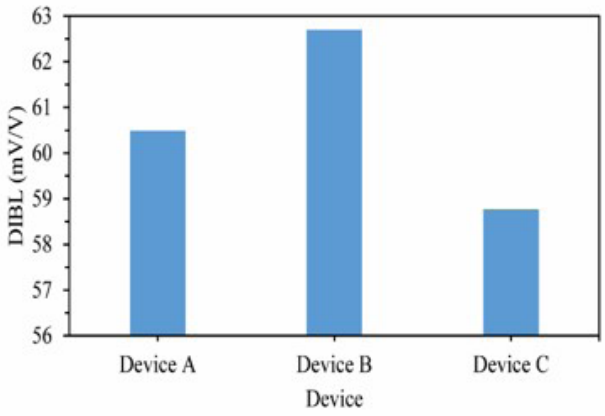

Figure 6: Comparison of DIBL in three devices.

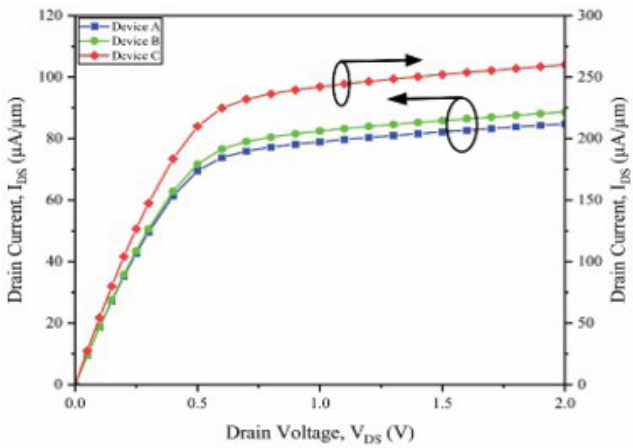

Figure 7: The output characteristics I_D vs V_{DS}.

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Conflict of Interest

None.

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