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Research Article

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Reliability Study of Highly Sensitive Nanoscale Dynamic Comparators Over a Wide Range of V_{DDs}/Temperatures for Future Flash/SAR ADCs

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Abstract

SAR (Successive approximation register)/Flash ADCs (Analog to digital converters) are the most important circuits used in a wide range of applications such as image sensing, data storage, ultrasound image, neural recording, wireless communication systems, serial link transceivers, industry healthcare, biosensing, and sensor networks and sensor readout circuits in Internet of Things. Dynamic comparators having ultra low kickback noise and power consumption, high speed, good power efficiency, excellent reliability, low offset voltage, supreme area efficiency, rail to rail output swing are the heart of these SAR/Flash ADCs. The noise/glitches, power consumption, speed and reliability of these comparators depends on V_{DD} and temperature variations. Here, we report the performance comparison of single-stage strong ARM, two stage double tail and three stage triple latch feed forward dynamic comparators under wide V_{DD}/temperature variations implemented with 16 nm CMOS.

Keywords

Analog to digital converters, CMOS technology, Internet of things, Successive approximation register, Wireless communication systems

Introduction

Speed, reliability, kickback noise, power consumption, area and power efficiency, offset voltage and rail to rail output swing are the key concerns that need to be taken care while designing and manufacturing SAR/Flash ADCs [1-4]. The power efficiency of SAR/Flash ADCs has been improved by more than 1000 times in the last 20 years as a result of numerous circuit and design advancements. Besides speed, reliability, and power efficiency, the compactness is also a serious concern for emerging applications such as image sensing, data storage, ultrasound image, neural recording, wireless communication systems, serial link transceivers, industry healthcare, biosensing and sensor networks and sensor readout circuits in Internet of Things where an array of SAR/Flash ADCs are the key requirements [5-7]. Low kickback noise, high speed, low offset voltage and power efficient dynamic comparators are the heart of SAR/Flash ADCs for the above highlighted applications. Moreover, comparators with ultra low power consumption and noise are highly preferable for the manufacturing of SAR/Flash ADCs for future implantable biosensing applications [8-10]. Technology scaling enables dynamic comparators one of the most exciting architectures to be adopted in future high performance and highly reliable SAR/Flash ADCs due to its predominantly digital architecture [11-17]. Moreover, dynamic comparators do not suffer from static power, that is, they offer zero static power. The offset voltage and noise of dynamic comparators are strongly depending on the V_{CM} (common-mode input voltage) and operating temperature of the comparators

[18-20]. Hence, here we investigate the V_{DD} and temperature variations on the performance and reliability of single-stage strong ARM, two stage double tail and three stage triple latch feed forward dynamic comparators using SPICE tools designed with 16 nm CMOS process.

Experimentation

Single stage strong arm comparator (SSSAC)

The SSSAC comparator based on pre-amplifier/latch consist of a tail transistor as current source, two-cross coupled inverter pairs, a clocked differential pair and four transistors for reset operation (Figure 1) [19].

Two stage double tail comparator (TS-DTC)

The partitioned input-latch TS-DTC was developed to overcome the constraints of a single current controlling both latching and integration, as well as to mitigate device stacking [20]. Because of the lesser transistor stacking, this architecture can operate more efficiently at lower V_{DDs}. The TS-DTC circuit consists of a pre-amplifier stage and a latch stage. Two reset transistors, a tail transistor current source at the bottom and a clocked differential pair form the pre-amplifier stage of the TS-DTC (Figure 2). The latch stage of TS-DTC circuit consists of a tail transistor current source on top, two cross-coupled pairs of inverters and an intermediate differential amplifier.

Three stage triple latch feed forward comparator (TS-TLFF)

The TS-TLFF dynamic comparator (Figure 3) consists of three stages-two amplifier/latch stages and a final latch stage. The first stage is formed by a differential amplifier (M_{1N}/M_{1P}), a NMOS-based half latch (M_{2N}/M_{2P}) and a clocked NMOStail transistor current source and the second stage is obtained by integrating an amplifier (M_{12N}/M_{12P}) with a PMOS-half latch (M_{4N}/M_{4P}) and an inverted clocked tail transistor current source. The final stage includes an NMOS latch (M_{5N}/M_{5P}), a clocked transistor tail current source, a feed forward (FF) path (M_{13N}/M_{13P}) and reset/transconductor devices M_{23N}/M_{23P} and M_{12N}/M_{12P} and a clocked pair M_{6N}/M_{6P} (refer [18]).

Results and Discussion

Single stage strong arm comparator (SSSAC)

In the reset phase of SSSAC operation (CLOCK = 0), the tail current source transistor turns OFF and the four reset transistors pull the output nodes (Op and On) to V_{DD} (Figure 4). When CLOCK switches to V_{DD}, the tail current source transistor turns ON and if the ΔV_{in} = Vp-Vn is positive, Op node remains at V_{DD} and "On" node discharges to zero potential (Figure 4 and figure 5). On the other hand, if ΔV_{in} = Vp-Vn is negative, the Op node discharges to zero potential and "On" node remains at V_{DD} (Figure 4). The SSSAC circuit showcased a P_{SC} (Short circuit power) of 64 - 78 µW at a variation in temperature (T) of 27 °C to 107 °C (Figure 6).

The SSSAC circuit implemented with a supply (V_{DD}) of 0.7 V (1.2 V) showcased a power consumption of 20.19 µW (306 µW) and 17.95 µW (241.1 µW) at a T of 27 °C and 107 °C, respectively. The SSSAC circuit implemented with a supply (V_{DD}) of 0.7 V (1.2 V) showcased a reduction in power consumption of 11.09% (21.21%) for a T variation from 27 °C to 107 °C. The SSSAC circuit implemented with a supply (V_{DD}) of 0.7 V (1.2 V) showcased a delay of 911.3 pS (903.5 pS) and 915.5 pS (906.3 pS) at a T of 27 °C and 107 °C, respectively. The SSSAC circuit operated at a T of 27 °C (107 °C) showcased an increase in power consumption of 15.15 times (13.43 times) for a V_{DD} variation from 0.7 V to

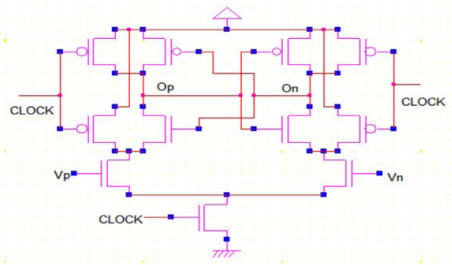

Figure 1: SSSAC comparator circuit [19].

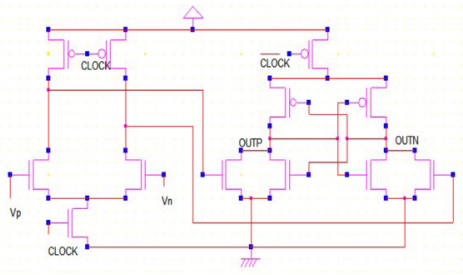

Figure 2: TS-DTC comparator circuit [20].

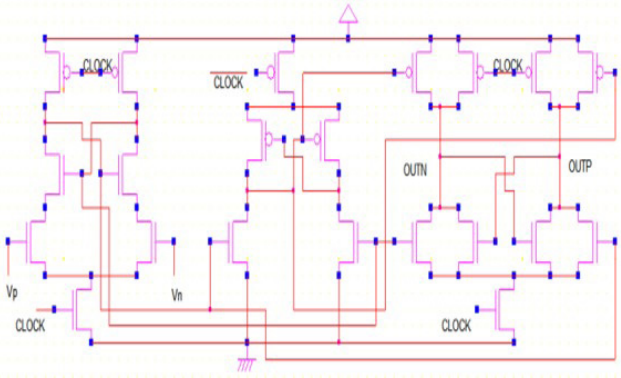

Figure 3: TS-TLFF comparator circuit [18].

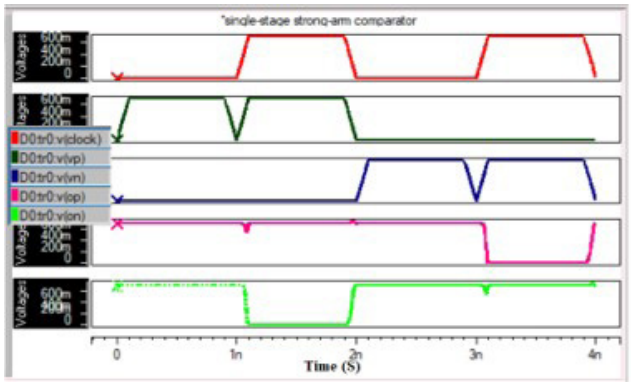

Figure 4: Transient analysis of SSSAC comparator circuit.

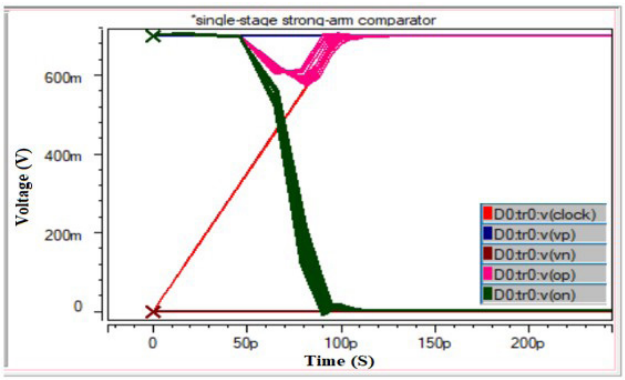

Figure 5: Variation in delay of SSSAC circuit with temperature.

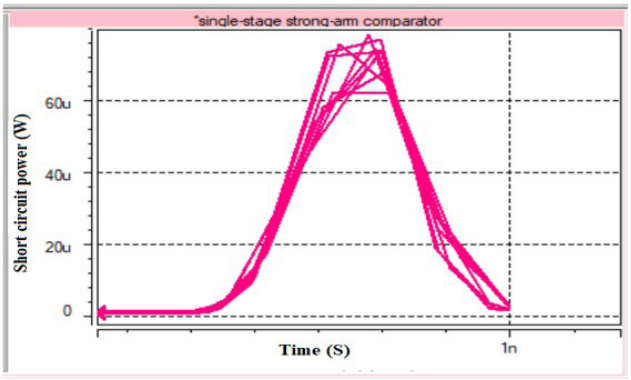

Figure 6: Variation in P_{SC} of SSSAC circuit with temperature.

1.2 V. The SSSAC circuit operated at a T of 27 °C (107 °C) showcased a reduction in delay of 0.86% (1.11%) for a V_{DD} variation from 0.7 V to 1.2 V. The SSSAC circuit operated with a ΔV_{in} of 0.7 V (0.1 V) showcased an increase in power consumption of 18.8% (21.38%) for a T variation from 27 °C to 107 °C. However, ΔV_{in} variation has not made any major change in the delay of SSSAC circuits at all operating temperatures (Figure 7).

However, due to the higher voltage overhead required by more number of vertically stacked transistors, its operation has not scaled as well into low VDD nanoscale nodes. Furthermore, due to its single current branch, this SSSAC circuit's noise/offset and speed are unfavourably dependent on the ΔVin.

Two stage double tail comparator (TS-DTC)

In the reset phase (CLOCK = 0), the transistors M_{2N} ans M_{2P} will turn ON and the nodes X+ and X- will be charged to V_{DD}. Therefore, the transistors M_{3P} and M_{3N} will turn ON and the output nodes (OUTP and OUTN) are discharged to zero potential. When CLOCK switches to V_{DD}, the transistors M_{2N} and M_{2P} will turn OFF. In this condition, if ΔV_{in} = Vp-Vn is positive, the OUTP node will be charged to V_{DD} and OUTN node will be discharged to zero potential. On the other hand, if ΔV_{in} = Vp-Vn is negative, the OUTP node will be discharged to zero potential and OUTN node will be charged to V_{DD} (details are in [18, 20]) (Figure 8 and figure 9). Complementary transistors are used as tail current sources in pre-amplifier and latch stages. The TS-DTC circuit showcased a P_{SC} (Short circuit power) of 150 - 260 µW at a variation in operating T of 27 °C to 107 °C (Figure 10).

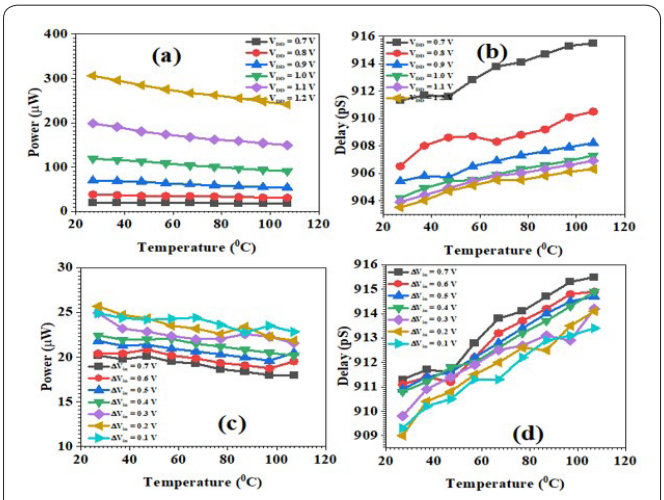

Figure 7: Effect of T, V_{DD}, and ΔV_{in} variations on SSSAC performance.

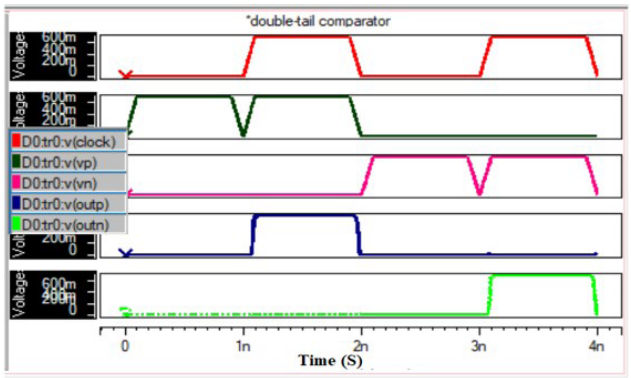

Figure 8: Transient analysis of TS-DTC comparator circuit.

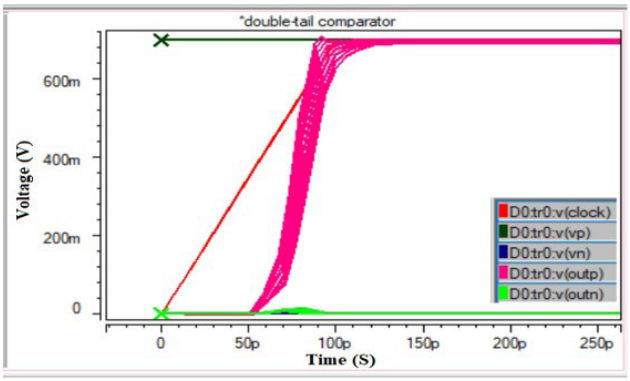

Figure 9: Variation in delay of TS-DTC circuit with temperature.

The TS-DTC circuit implemented with a supply (V_{DD}) of 0.7 V (1.2 V) showcased a power consumption of 47.66 µW (624.4 µW) and 39.52 µW (508.1 µW) at a T of 27 °C and 107 °C, respectively. The TS-DTC circuit implemented with a supply (V_{DD}) of 0.7 V (1.2 V) showcased a reduction in power consumption of 17.1% (18.63%) for a T variation from 27 °C to 107 °C. The TS-DTC circuit implemented with a supply (V_{DD}) of 0.7 V (1.2 V) showcased a delay of 24.2 pS (5.681 pS) and 34.54 pS (9.252 pS) at a T of 27 °C and 107 °C, respectively. The TS-DTC circuit operated at a T of 27 °C (107 °C) showcased an increase in power consumption of

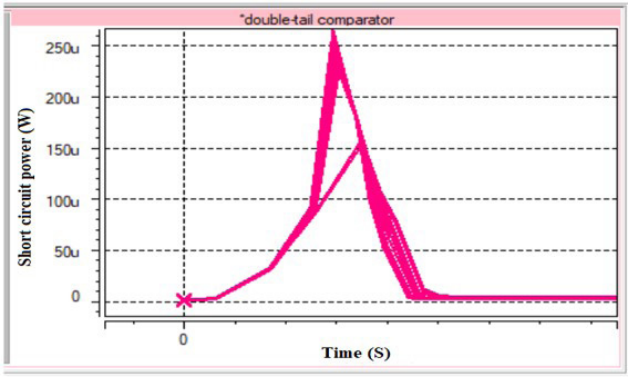

Figure 10: Variation in P_{SC} of TS-DTC circuit with temperature.

13.10 times (12.86 times) for a V_{DD} variation from 0.7 V to 1.2 V. The TS-DTC circuit operated at a T of 27 °C (107 °C) showcased a reduction in delay of 66.65% (73.21%) for a V_{DD} variation from 0.7 V to 1.2 V. The TS-DTC circuit operated with a ΔV_{in} of 0.7 V (0.1 V) showcased a decrease in power consumption of 17.08% (13.06%) for a T variation from 27 °C to 107 °C. The TS-DTC circuit operated with a ΔV_{in} of 0.7 V (0.1 V) showcased an increase in delay of 29.94% (30.99%) for a T variation from 27 °C to 107 °C. At constant T, TS-DTC circuit with less ΔV_{in} showcased higher power consumption and delay (Figure 11).

The TS-DTC circuit offered an outstanding resolution of upto 5 mV. However, it is noted that when ΔV_{in} is reduced from 700 mV to 5 mV, the TS-DTC circuit produces more glitches (Figure 12, figure 13, figure 14, and figure 15). These glitches lead to increased power consumption and delays.

Three stage triple latch feed forward comparator (TS-TLFF)

In the reset phase (CLOCK = 0), the output nodes Op and On are pushed to V_{DD}. When CLOCK = 1, if ΔV_{in} = Vp-Vn is positive, the Op node will be charged to V_{DD} and On node will be discharged to zero potential. On the other hand, if ΔV_{in} = Vp-Vn is negative, the Op node will be discharged to zero potential and On node will be charged to V_{DD} (details are in [18]) (Figure 16 and figure 17). The TS-TLFF circuit showcased a P_{SC} of 250 - 350 µW at a variation in operating T of 27 °C to 107 °C (Figure 18).

The TS-TLFF circuit implemented with a supply (V_{DD}) of 0.7 V (1.1 V) showcased a power consumption of 54.1 µW (479.1 µW) and 46.23 µW (400 µW) at a T of 27 °C and 107 °C, respectively. The TS-TLFF circuit implemented with a supply (V_{DD}) of 0.7 V (1.1 V) showcased a reduction in power consumption of 14.55% (16.51%) for a T variation from 27 °C to 107 °C. The TS-TLFF circuit implemented with a supply (V_{DD}) of 0.7 V (1.1 V) showcased a delay of 21 pS (2.977 pS) and 28.06 pS (3.004 pS) at a T of 27 °C and 107 °C, respectively. The TS-TLFF circuit operated at a T of 27 °C (107 °C) showcased an increase in power consumption of 8.86 times (8.65 times) for a V_{DD} variation from 0.7 V to 1.1 V. The TS-TLFF circuit operated at a T of 27 °C (107 °C) showcased a reduction in delay of 85.82% (89.29%) for a V_{DD} variation from 0.7 V to 1.1 V. The TS-TLFF circuit operated

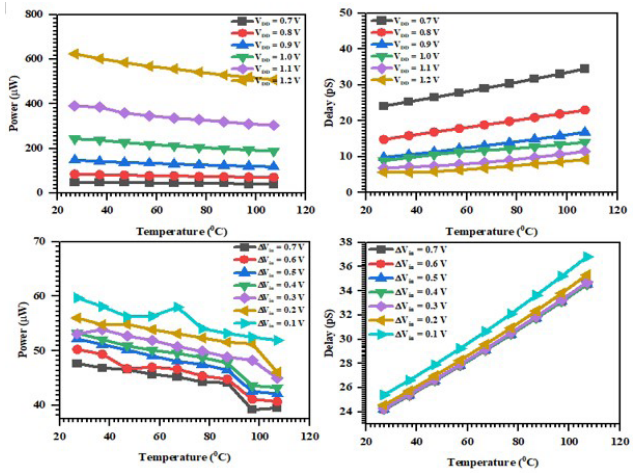

Figure 11: Effect of T, V_{DD}, and ΔV_{in} variations on TS-DTC performance.

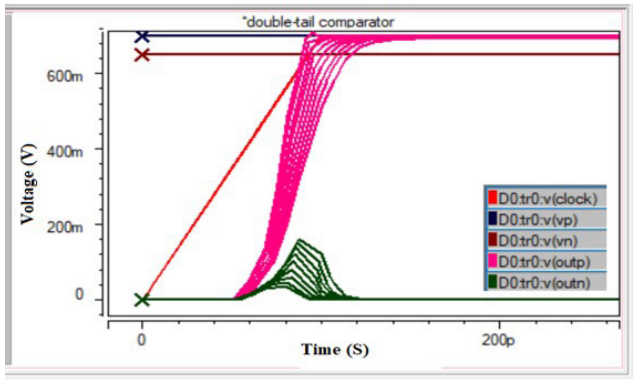

Figure 12: Transient analysis of TS-DTC circuit with ΔV_{in} = 50 mV.

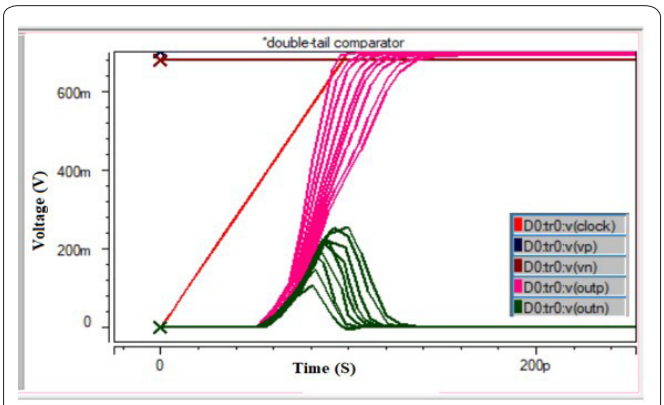

Figure 13: Transient analysis of TS-DTC circuit with ΔV_{in} = 20 mV.

with a ΔV_{in} of 0.7 V (0.1 V) showcased a decrease in power consumption of 14.55% (16.51%) for a T variation from 27 °C to 107 °C. The TS-TLFF circuit operated with a ΔV_{in} of 0.7 V (0.1 V) showcased an increase in delay of 25.16% (23.12%) for a T variation from 27 °C to 107 °C. At constant T, TS-TLFF circuit with less ΔV_{in} showcased higher power consumption and delay (Figure 19).

Conclusion

While information/data is increasingly being processed

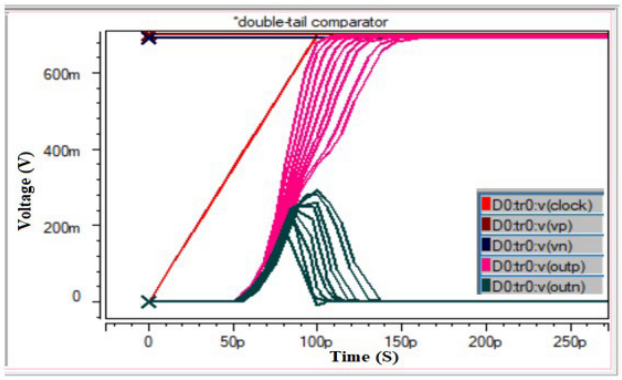

Figure 14: Transient analysis of TS-DTC circuit with ΔV_{in} = 10 mV.

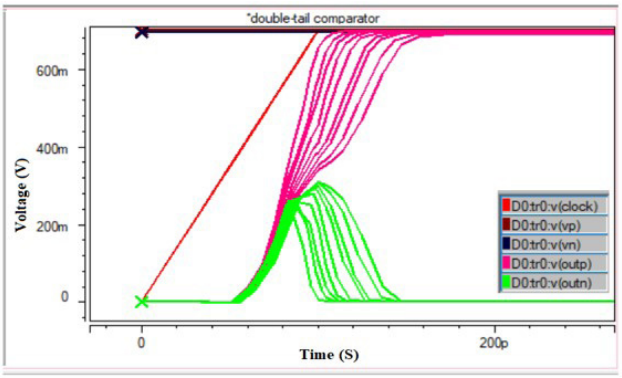

Figure 15: Transient analysis of TS-DTC circuit with ΔV_{in} = 5 mV.

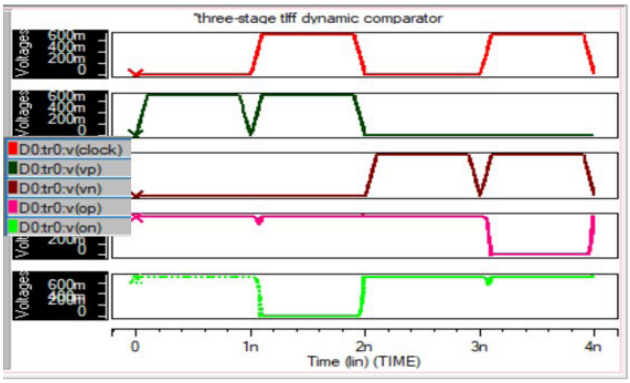

Figure 16: Transient analysis of TS-TLFF comparator circuit.

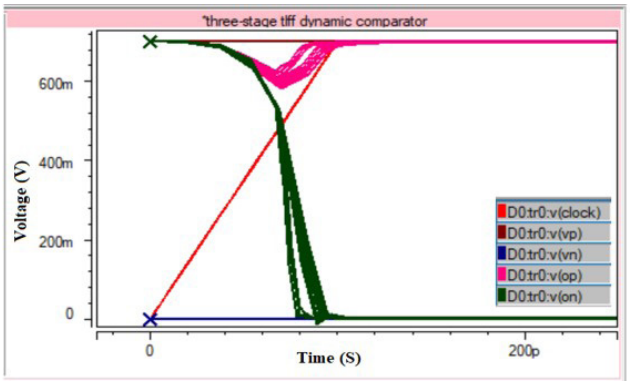

Figure 17: Variation in delay of TS-TLFF circuit with temperature.

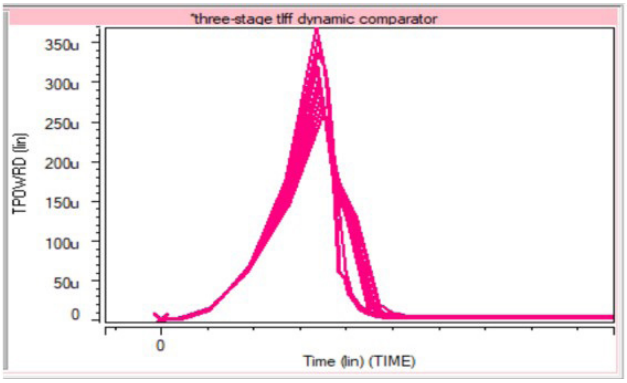

Figure 18: Variation in P_{SC} of TS-TLFF circuit with temperature.

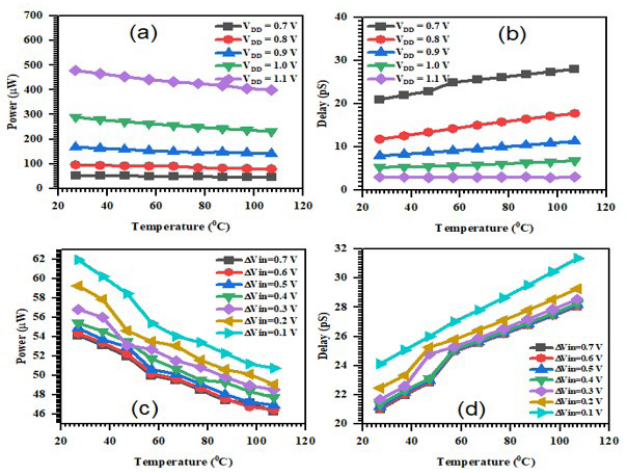

Figure 19: Effect of T, V_{DD}, and ΔV_{in} variations on TS-TLFF performance.

digitally, the physical world continues to remain analogue. When these two domains meet, as in data storage, wireless/wireline communication and a wide variety of sensor applications, we need to convert analogue and digital signals. Therefore, ADCs are critical components in nearly all electronic systems and comparators are the vital blocks present in ADCs and the ADC performance purely depends on comparator performance. The reliability of ADC also depends on reliability of comparators. In this work, we investigated the reliability and V_{DD} scaling effects on the comparators (SSSAC, TS-DTC and TS-TLFF) performance. At 27 °C, SSSAC, TS-DTC and TS-TLFF comparators showcased a power consumption of 20.19 µW, 47.66 µW and 54.1 µW, respectively, whereas, at 107 °C, SSSAC, TS-DTC and TS-TLFF comparators exhibited a power consumption of 17.95 µW, 39.52 µW and 46.23 µW, respectively. Similarly, at 27 °C, SSSAC, TS-DTC and TS-TLFF comparators showcased a delay of 911.3 pS, 24.2 pS and 21 pS, respectively, whereas, at 107 °C, SSSAC, TS-DTC and TS-TLFF comparators showcased a delay of 915.5 pS, 34.54 pS and 28.06 pS, respectively. These comparators are found to be highly efficient in comparing signals up to a ΔV_{in} of 10 mV.

Acknowledgements

None.

Conflict of Interest

None.

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