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Response Analysis of a Polysilicon-NADGFET Inverter with High-k and Low-k Gate Oxide Materials at Sub-90 nm Regime: A TCAD Simulation

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Abstract

In this paper response from an inverter at sub-90 nm regime, comprising of non-aligned double gate field effect transistors (NADGFETs) have been presented by replacing a gate oxide layer with the silicon dioxide (low-k, dielectric constant 3.8), and hafnium dioxide (HfO_2) (high-k, dielectric constant 24). The simulation results are presented using a 2-Dimensional simulation in TCAD environment. The transient response, current consumption, and voltage transfer characteristics (VTC) are presented along with the total power dissipation. The inverter is applied with extreme high frequency i.e., 10 GHz, and has load capacitor of 10 femto-Farad value. It is observed that inverter gives rise time, fall time with low-k gate oxide as, 14.5 picosecond (ps), 7.89 ps, and with high-k gate oxide as, 16.3 ps, 8 ps, respectively. The total power consumption is 0.463 mW, and 0.525 mW, for low-k and high-k gate oxide, respectively. The VTC shows the same switch point for the two gate oxides, hence the low-k material can be suitable gate oxide for a logic gate meant to work at extreme high frequencies.

Keywords

Double gate, Dielectric constant, NADGFET, Power consumption, Transient response, Voltage transfer characteristics

Introduction

Low power and high packing density of integrated circuits coupled with increased computation power has led to a successful increase in the demand of nano devices in the semiconductor industry. The constant scaling of semiconductor devices has led to their entry into the sub-100 nm regime. Nevertheless, numerous short channel effects (SCEs) are in spotlight as a result of the device aggressive scaling in dimensions. For a better switching characteristic from a semiconductor device, the need for good control over a channel is required, the multi-gate design is a successful strategy for overcoming these SCEs [1]. Different hybrid topologies, such as the double gate (DG), triple gate, and gate all around (multi-gate) metal oxide semiconductor field effect transistors (MOSFETs), were developed according with the device specification to lower the SCEs.

The design of a nano device needs specific design rules in order to scale the device dimension. A better way to design could be by examining the 2D field effects within the nano transistor structure, which can help to determine the smallest gate length that can control the channel within the generation of technological advancement. The device design is frequently carried out through computation using sophisticated 2D modeling software. A comparison of the first-order analytical estimation along with the computational model determines the possible modification needed in the device design. This can be carried out with more rigorous iterations in device design that can obey scaling as per design standards thereby increasing the packing density in the design of digital

and analog circuits. Recent research has developed a number of device design techniques to improve the effectiveness of re-sized devices while decreasing SCEs and preserving electrical characteristics. Currently, most design discusses junctionless symmetric and asymmetric undoped device operating with a common gate controlling the flow of current from drain to source.

The presented work in this paper advances the device design by proposing a doped junction symmetric structure with non-align gates that effectively controls the switching characteristics of the nano device. A DGMOSFET controlling an electrical doped channel bounded by the gate electrodes on both side of the device, gives better control on channel segment placed close to the double gates. This can help to control a substantial amount of current flowing through the channel. Hence, in this work a symmetrical junction non-aligned polysilicon-based DGMOSFET with n-channel (NADGNFET), and p-channel (NADGPFET) [2, 3], is used to design an inverter structure to evaluate the response at nanoscale design. To test the capability of sub-100 nm devices, inverter is a very popular configuration to evaluate the measurement results. The result given by the inverter configuration can gives a better insight to the researcher working with the device performance at radio frequency and beyond [4].

In this paragraph, some results from inverter configuration using nano-devices are reviewed and presented. The work in [5], have developed a compact Schottky based inverter which needs dedicated process and the requirement to have other digital devices cannot be fulfilled because of dedicated process fabrication steps. However, the authors have shown improved response over the conventional CMOS based inverter at high frequency range. An inverter logic gate using a 10-nm double gate-all-around transistor with asymmetric channel width is proposed in [6], the main challenge is to control the amount of variation to form asymmetric transistors during the fabrication process. The configuration was tested without load capacitor and shown to give improved response at ultra-high frequency range, and improved power dissipation compared to a symmetrical gate-all-around nanotube. A recessed silicon channel double gate junctionless field effect transistor of 20 nm length has been proposed in [7], and inverter simulation shows that it can achieve steep voltage transfer characteristics, however the work do not provide much detail about the transient simulation set-up and power dissipation of the inverter. A vertical stacked transistor is proposed in [8], to scale down the inverter design to sub-40 nm gate length. The process needs work function adjustment in p-type device. Therefore, the present work will explore the polysilicon material instead of metal layer to overcome process related adjustment which may reduce the fabrication cost.

The layout of this paper is as follows: Section II presents the design of a polysilicon based NADGFET inverter, and test condition along with measurement set-up. Section III discusses the proposed inverter response using two different dielectric constant material in the gate oxide. Section IV presents inverters static characteristics along with measured parameter. Finally, in Section V, the conclusions are drawn and presented.

Experimentation

Polysilicon-based inverter design using NADGFET devices

Figure 1 shows a polysilicon-NADGFET (poly-NADGFET). The inverter consists of NADGPFET and NADGNFET devices. The 50% non-alignment in 90 nm device makes the total length 180 nm. One end of source is connected to V_{DD} and other to ground. The drain of two devices are in contact to which the load capacitor is connected, the output is measured across it. The increased area of drain reduces R_{SD} resistance, improving the inverter performance [4]. The 15 nm is taken as thickness of the device, the polysilicon gate has thickness of 1.5 nm, and gate oxide layer of 1 nm is given with silicon dioxide, SiO_2 (k = 3.8, low-k), and HfO_2 (k = 24, high-k), the other device specifications are given in table 1. For simplicity the wiring connections are not shown in figure 1. A common side of the gate is connected with V_{IN} i.e., input signal, through which an extremely high clock frequency with specification given in table 2 is applied. The clock signal swings between V_{DD} = 1 V (supply voltage), and 0 V (ground). The 10 femto-Farad load capacitor is chosen according to the standard requirement from fan-out [4]. The clock in table 2 has 50% duty cycle, where T_d is the delay time, T_r is the rise time, and T_f is the fall time. The frequency f = 1/T, is also specified for each time specification, 1p = 10^{-12}, and 1 G = 10^9.

This paper uses 2D-Sentaurus Device Simulator for a simulation test of the proposed poly-NADGFET inverter. All the design parameters and voltages are selected according to the International Technology Road Map for Semiconductors [9]. The device parameters for the NADGNFET have I_{ON}/

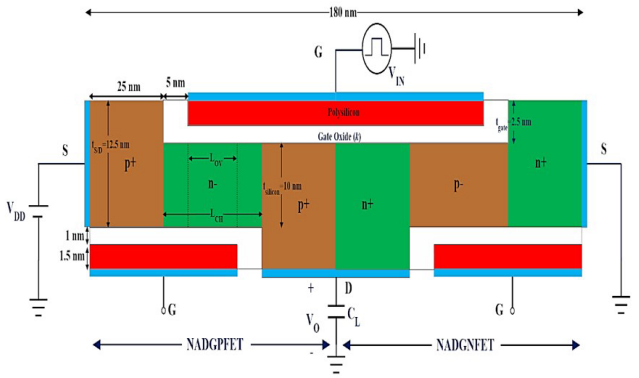

Figure 1: The poly-NADGFET based inverter. The supply voltage V_{DD} = 1 V, and V_{IN} is the input voltage from a clock signal, and V_O is the observed output. All the gates are applied with the same voltage, and C_L is the load capacitor.

Table 1: The device specifications.

Device	NFET	PFET
Donor conc. (cm^{-3})	10^{18}	10^{12}
Acceptor conc. (cm^{-3})	10^{12}	10^{18}
L_{CH} (nm)	40	40
L_{OV} (nm)	30	30
t_{gate} (nm)	2.5	2.5
$t_{silicon}$ (nm)	10	10

Table 2: The clock specifications used in simulation.

Time/Frequency	Extreme high
T_d (sec)/f_d (Hz)	1 p/10^3 G
T_r=T_f (sec)/f_r (Hz)	1 p/10^3 G
T_{ON} (sec)/f_{ON} (Hz)	50 p/20 G
T(sec)/f(Hz)	100 p/10 G
C_L (fF)	10

I_{OFF} value for SiO_2 as 0.98 x 10^8, and HfO_2 as 0.24 x 10^9. The measured drain induced barrier lowering for SiO_2 is 12.22 mV/V, and HfO_2 is 6.11 mV/V; the sub-threshold swing for SiO_2 is 62 mV/decade and HfO_2 is 60 mV/decade. The intrinsic gain with SiO_2 is 82.5 V/V and with HfO_2 is 164.4 V/V [10]. The f_T (cut-off frequency) for SiO_2 is 109.7 GHz, and for HfO_2 is 55.8 GHz, owing due to total gate capacitance, C_{GG} = 2.72 fF, and 6.19 fF, for low-k, and high-k gate oxide material, respectively, as discussed in [10].

Results and Discussion

Inverter's transient response and power consumption

The transient response from the inverter simulation is presented in this section. Figure 2, and figure 3 show the device response to the applied extreme high frequency (EHF). From figure 2, the measured value of propagation delay @0.5V_{DD} for a low-k gate oxide inverter comes to be t_{pr} =14.5 ps, t_{pf} = 7.89 ps [2], where t_{pr} is propagation delay rise-time, and t_{pf} is propagation delay fall-time. Figure 3 gives t_{pr} = 16.3 ps, t_{pf} = 8 ps, for a high-k gate oxide inverter. The propagation delay frequency (f_d) can be calculated using equation 1.

$$f_d = \frac{1}{0.5 \text{ x } \left(t_{pr} + t_{pf}\right)} \quad (1)$$

The propagation delay frequency for SiO_2, and HfO_2 inverter is estimated to be 89.32 GHz, and 82.30 GHz, respectively. The SiO_2 inverter gives ±6% overshoot and undershoot compared to ±18% overshoot and undershoot given from a HfO_2 inverter. Close inspection of figure 2, and figure 3, gives the reason for the lower propagation delay frequency in high-k oxide inverter. Even though the amount of I_{ON} current determines the device can charge and discharge the total capacitance i.e., parasitic and load capacitance. An increased parasitic capacitance strongly affects the propagation delay, with the exception in low-k oxide material which give low value of parasitic capacitance. The NADGPFET device takes a long time to charge due to its hole mobility determines the I_{ON} current rather than the electron mobility in NADGNFET device. Even with a high I_{ON}/I_{OFF} ratio, unless the I_{ON} is sufficiently high, the inverter may not perform well in transient response.

Figure 4 shows the propagation delay frequency vs load capacitor plot, with the decreased value of load capacitor the f_d increases, thereby the transient response of the inverter improves. The SiO_2 based inverter shows a better response compared to the HfO_2 based inverter. Figure 5, and figure 6, show the transient response at radio frequency (RF), i.e., 100 MHz, T = 10 nsec. The figure shows a good response by the inverter with a load capacitor of 10 femto-Farad, hence the inverter works good at RF.

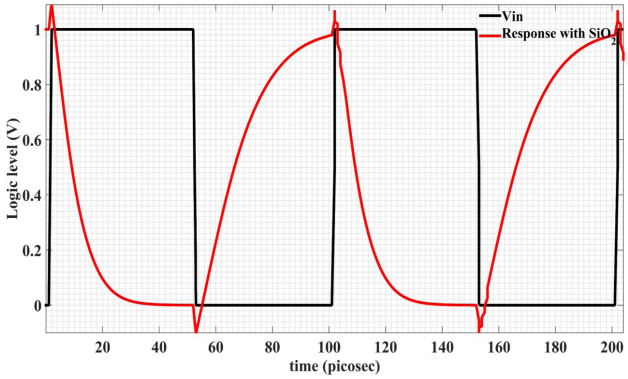

Figure 2: The SiO_2 poly-NADGFET inverter response at EHF.

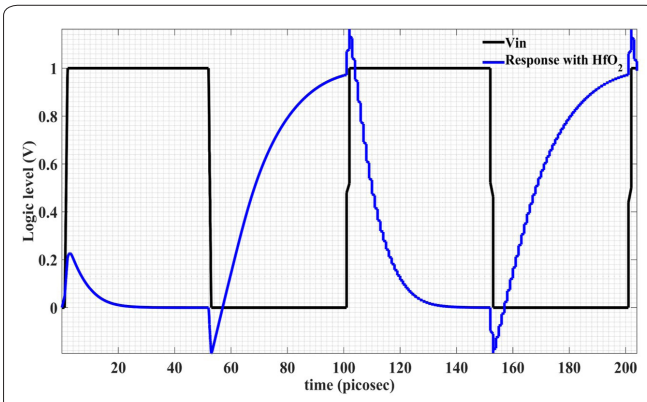

Figure 3: The HfO_2 poly-NADGFET inverter response at EHF.

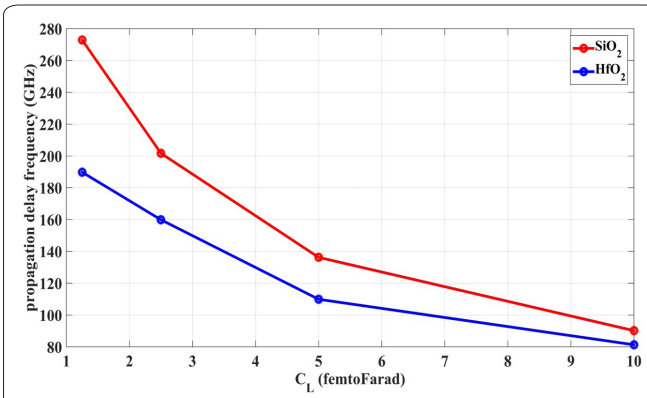

Figure 4: The f_d variation with C_L at EHF.

Figure 7, and figure 8, show the current consumption by the inverter with two gate dielectric materials at EHF. The figure shows dynamic charge transfer from the supply voltage to the load capacitor and then to the ground. The static power consumption (P_{static}) is found to be ≈ 1 nW. The peak value of current for SiO_2 inverter is 1.2 mA, whereas for HfO_2 inverter is 2.3 mA. The reason can be given to high total gate capacitance in HfO_2 due to increased value of dielectric constant. The total power consumption is given by equation 2.

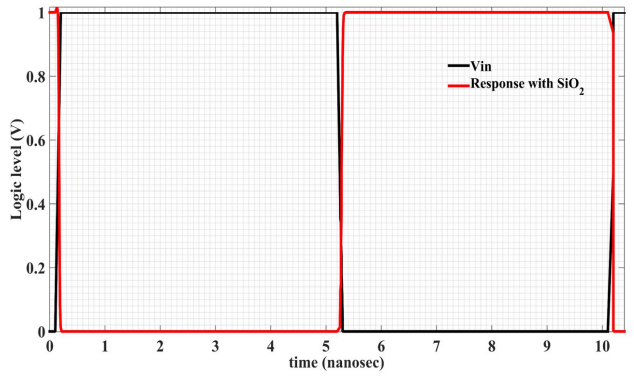

Figure 5: The SiO_2 poly-NADGFET inverter response at RF.

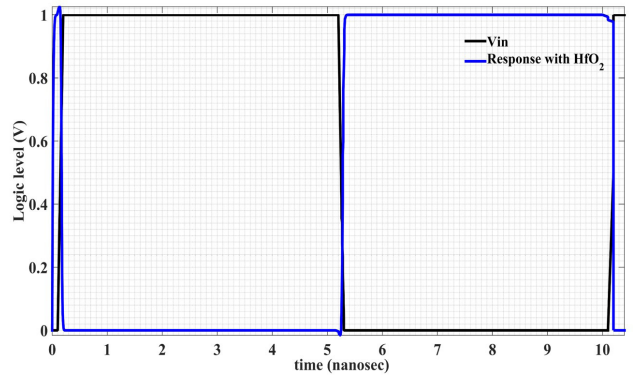

Figure 6: The HfO_2 poly-NADGFET inverter response at RF.

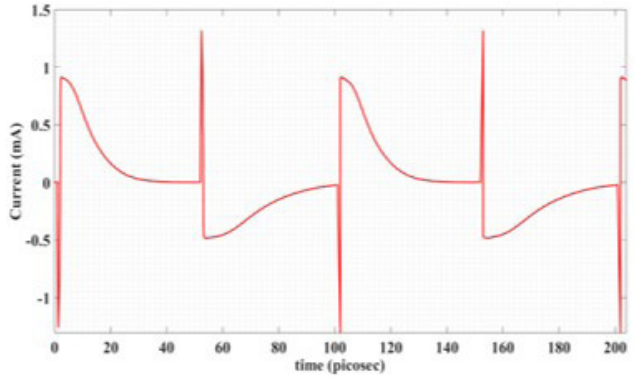

Figure 7: The current variation across load capacitor for SiO_2 inverter.

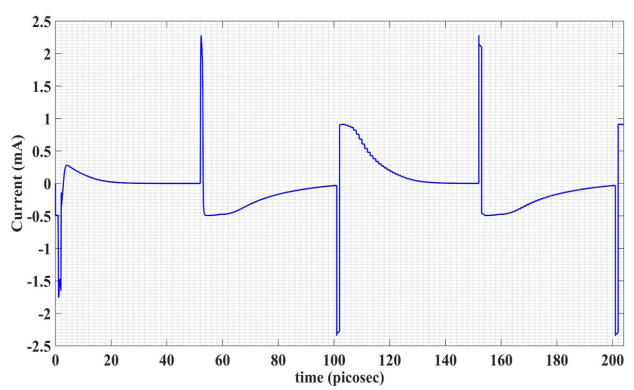

Figure 8: The current variation across load capacitor for HfO_2 inverter.

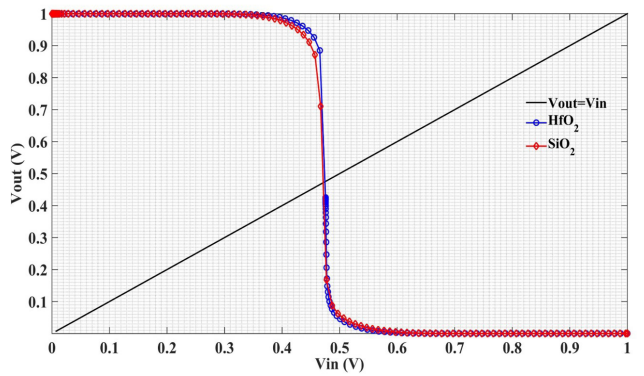

Figure 9: The inverter VTC for two dielectrics, i.e., low-k and high-k constant.

$$P_{total} = P_{static} + C_{eff} \text{ x } f_d \text{ x } V_{DD}^2 \quad (2)$$

In equation 2, the effective gate capacitance i.e., $C_{eff} = C_{GG} + C_L$ Farad. The calculated value of total power consumption for SiO_2 inverter is 0.463 mW, whereas for HfO_2 inverter is 0.525 mW. The next section presents the voltage transfer curve of the inverter for the two dielectric materials in the gate oxide.

Inverter's static characteristics

This section discusses the measured VTC of the poly-NADGFET inverter with two gate oxide material. The aspect ratio and threshold voltage of the devices plays a significant role in determining the switch point (V_{sp}) voltage of an inverter. From design requirement, it is desirable in an inverter to show the switch point at mid of the supply voltage, however this may change with process variation. Figure 9 shows the VTC curve of the inverter. The estimated value of V_{sp} = 0.4753 V, which is close to half of supply voltage. The response demonstrates that the inverter operates effectively at switch points when switching from high to low voltage level. The advantage of a polysilicon layer is its uniform work-function which makes a threshold voltage variation less on NADGNFET and NADGPFET devices, irrespective of gate oxide. The measured value of inverter gains for SiO_2 is 16.88 V/V, and for HfO_2 is 98.25 V/V, the high gain for HfO_2 is due to its high-k, that increases the transconductance of the device [10].

Conclusion

In this work an inverter using poly-NADGFET devices is presented. The simulation of the device was done in a 2D TCAD environment. The inverter gate oxide was emulated with low-k and high-k dielectric material. The advantage of using polysilicon in sub-100 nm design is its low cost in fabrication and work-function matching, resulting in a stable switch point voltage irrespective of gate oxide. Even though high-k oxide increases inverter gain, due to the increased value of parasitic capacitance, its influence is seen in decreased propagation delay frequency and increased power dissipation.

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Conflict of Interest

None.

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