Nano World Journal

https://doi.org/10.17756/nwj.2021-091

Research Article

Open Access

Quantum Switching Modeling and Optimization of a Metal-Oxide-Semiconductor Gated Y-Shaped Structure

Trevor McDonough[1*], Vladimir Mitin[1], Vadim Tokranov[2], Michael Yakimov[2], and Serge Oktyabrsky[2]

[1]*Department of Electrical Engineering, SUNY University at Buffalo, USA*

[2]*Department of Nanoscience, SUNY Polytechnic Institute at Albany, USA*

[*]Correspondence to:
Trevor McDonough
Department of Electrical Engineering
SUNY University at Buffalo, USA
Tel: 1-716-645-1035
E-mail: trmcdono@buffalo.edu

Received: December 02, 2021
Accepted: January 04, 2022
Published: January 06, 2022

Citation: McDonough T, Mitin V, Tokranov V, Yakimov M, Oktyabrsky S. 2021. Quantum Switching Modeling and Optimization of a Metal-Oxide-Semiconductor Gated Y-Shaped Structure. *NanoWorld J* 7(4): 40-45.

Published by United Scientific Group

Abstract

Using Silvaco Atlas codes achieving 3D simulation by combining a 2D Schrodinger-Poisson electrostatic solver and non-equilibrium Green's function (NEGF) transport simulator, we demonstrated low-power switching in a gated Y-shaped one-dimensional ballistic waveguides prepared from Al-free InGaAs/GaAs quantum well. We have evaluated current switching in the devices as a function of modulation doping and temperature. Modulation doping was implemented symmetrically around the quantum well with 5 nm spacer layers to match the experimentally fabricated test structures. To verify the solver was correctly treating quantum transport, simulations were executed for different doping levels to control filling of the first few 1D subbands. The resulting conductance showed the expected stair-like profile with the quantum steps of 7.75×10^{-5} S. We demonstrated the current switching between branches of the Y-shaped waveguide at gate voltage as low as 10 mV with 1 mV bias applied to the waveguide, and compared these results to estimates based on the overlap of wavefunctions of the stem and the branches. Notably, the most efficient switching occurs when only the first subband of the stem was occupied with the second subband starting to fill near the junction. In this case, the conduction 1D subband discontinuity at the junction results in the first energy level of the branches matching the second partially filled subband of the stem. This results in one order of magnitude ballistic current steering between the degenerate (metallic) semi-conductor 1D branches at about 6 mV at low temperature.

Keywords

Y-branch switch, Quantum switch, Silvaco atlas, Heterostructure, Simulation

Introduction

The Y-branch switch (YBS) functions by shifting the wavefunction of electrons with an electric field to steer them down a desired branch, as shown in Figure 1. The YBS promises lower intrinsic capacitance, lower susceptibility to parasitic capacitance, lower switching voltage, and shorter delay time than a traditional metal-oxide-semiconductor field effect transistor (MOSFET) [1] while also being able to easily implement conventional logic gates [2-6] and open the door to reversible logic circuits [7]. A comparison between the theoretical switching parameters of an "ultimate" MOSFET and an YBS following the approach proposed in reference [1] can be seen in Table 1.

Although the YBS operation is based on different physics than that of junction or FETs it is worth comparing their basic parameters. For example, the difference for switching performance arises from ultimately low-voltage operation at

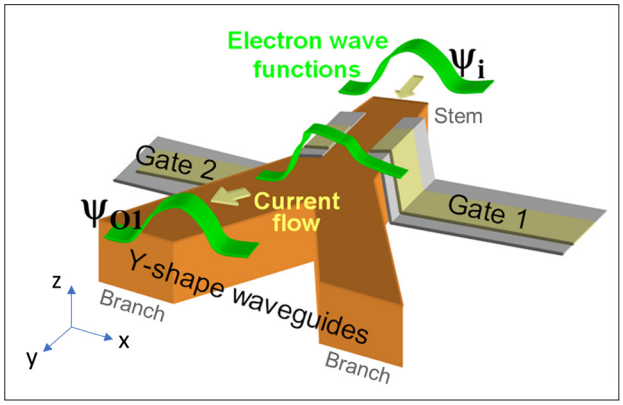

Figure 1: Schematic diagram of an YBS with MOS gates in operation. Electrons that are injected into the stem have their wavefunction perturbed by an electric field between the gates causing them to steer down the desired branch.

relatively high current specific for degenerate semiconductor or metallic 1D waveguides. A simple estimate following a framework outlined in reference [1] predicts an ultimate MOSFET will switch 20 electrons at 60 mV for ultimate bit switching energy of 1.2 eV at room temperature and for the on/off ratio I_{on}/I_{off}=10. Each of those 20 electrons being switched would then be needed to operate the next gate. By comparison, an YBS will steer 200 electrons at 6 mV but only about 10 electrons are needed for operation of the next device gate.

This illustrates one of potential benefits of YBS over FET, i.e. low intrinsic capacitance. In fact, the YBS gate capacitance is not related to the control of carrier concentration in the channel and gate oxide thickness, but rather to the static spacing between the gates – i.e. the waveguide width, and so can be significantly less than in a FET. This allows for significantly higher parasitic capacitance in a circuit, better impedance matching between the device and interconnects, and/or high fan-out while keeping power dissipation constant.

The switching of an YBS has already been successfully demonstrated using ridge [8] and Schottky [9] gates which suffer from low switching efficiency due to the relatively large air gap in the case of ridge gates and high leakage current in the case of Schottky gates. We expect that separating the metal gate from the waveguide with a high $-\kappa$ dielectric will greatly reduce leakage current while maintaining the high gate efficiency. Therefore, we set out to simulate an YBS implementing MOS sidewall gates using Silvaco Atlas before moving on to fabricate such a device.

In the process of simulating the devices, the energy band profile and carrier concentration were evaluated for the optimal operation of such devices. In short, the inherent geometry of a symmetric intersection results in the branches each having half the width of the stem. This dimensional ratio results in the alignment of the first energy level in the branches with the second level of the stem. When doped properly, the simulations show that band bending will result in the second level of the branches beginning to fill near the intersection, while only the first will be populated in the branches and the majority of the stem.

In this work, Y-branch switches implementing MOS sidewall gates were simulated and switching at low gate voltages was demonstrated. The ideal device geometry and doping fo such devices were also proposed.

Materials and Methods

Structure

All the simulations described in this paper were done using Silvaco Atlas for its mode-space NEGF solver to obtain solutions for 3D devices. Unless otherwise specified, all simulations described herein incorporated the following structure: a 10 nm thick $In_{0.2}Ga_{0.8}As$ quantum well with its center being set to z=0,

Table 1: Comparison between theoretical switching parameters of an "ultimate" MOSFET and an YBS. Select data adopted and calculated using approach in [1].

Parameter	"Ultimate" MOSFET	YBS
ΔV_{SW} required for I_{on}/I_{off}=10 (mV)	60	6
Maximum capacitance allowed for switching 1.2 eV (aF)	50	5000
Intrinsic capacitance per device (aF)	50	20
Current (μA)	16	2
Intrinsic switching delay (ps)	0.2	0.09
Delay with full 5fF parasitics (ps)	18	20
Electrons switched at ΔV_{SW} required for	20	200
Electrons needed to operate next gate I_{on}/I_{off}=10	20	10

sandwiched between GaAs. The full stack simulated spanned -30 nm≤z≤28 nm . Undoped 5 nm spacers above and below the well separated it from an 3 nm and 2 nm thick n-doped GaAs regions above and below the quantum well, respectively, which would then provide the well with charge carriers. The doping concentrations in these regions were always set to equal each other, but varied depending on the simulation, with the most promising doping of about $1x10^{17}$ cm^{-3}, which translates into total electron sheet concentration of $5x10^{10}$ cm^{-2} available in the structure. All other regions were left undoped.

It should be noted that in a real structure of these nano-scale dimensions, there would be just a few dopant atoms present at this concentration. Naturally, it is not an issue for the simulation with assumed uniform dopant charge distribution, but will result in variability of parameters in a real device due to fluctuations of doping similar to short-channel transistors [10]. Test devices however will likely suffer from some Fermi-level pinning and charges at the at the waveguide sidewall and will require higher modulation doping with less fluctuations. In any case, optimization would be needed in the real test structures.

Silvaco Atlas's NEGF solver was limited to 50 nm long structures in the direction of current (y-direction), constraining the stem to a length of 35 nm and the branches to a length of 15 nm. The stem was 60 nm wide, centered at x=0, and the branches were each 29 nm wide, spanning 1 nm≤|x|≤30 nm. The entire length (y) and depth (z) of the structure had a layer of Al_2O_3 spanning 30 nm≤|x|≤35 nm separating the waveguide from the gate contact. When the devices are eventually fabricated, the atomic layer deposition of this Al_2O_3 will also help clean and passivate the surface to improve the gate efficiency, and reduce variability of the devices [11-13].

The source and the drains were defined to be planes at y=25 nm and y=-25 nm, respectively. The NEGF solver required these contacts be defined implementing Neumann boundary conditions, which was accomplished with the "reflect" parameter in the contact definition. The gate contacts spanned the entire depth of the structure, extending from the branch-stem intersection (x=-15 nm) to x=15 nm. These gate contacts needed to use the default (Dirichlet) boundary conditions due to the presence of the dielectric, and therefore needed their work function calibrated such that the potential in the channel wasn't significantly affected by their presence.

Simulations

Confirming that Silvaco Atlas's NEGF solver was properly simulating quantum conductance was a critical step. As more 1D energy subbands are populated in a confined structure, the conductance should increase in a step-like fashion. More specifically, each additional mode increases the conductance by the conductance quantum, $G_0 = \frac{2e^2}{h} \cong 7.748\times10^{-5}\,\mathrm{S}$ where, e is the elementary charge and h is Planck's Constant [14, 15]. To observe the effects of individual subbands filling in our simulations, NEGF simulations were executed for the structure with numerous doping concentrations and a source-drain voltage of at V_{ds}=1 mV a temperature of T=10 K. The gate contacts were excluded in these simulations in order to avoid the need to calibrate the work function for each doping concentration applied.

Before running the full simulations, estimates were made to which the final simulation results could be compared. For these estimates, 2D Schrödinger-Poisson solutions of cross-sections were taken of our waveguides of varying widths (in this case, 60 nm for the stem and 30 nm for the branches) and gate voltages were applied across the stem. Figure 2 shows how a 1D slice of the ground-state wavefunction-map in the gate-region was shifted with an increasing voltage. The overlap integrals of these shifted wavefunctions in the stem and the wavefunction in each branch were then calculated to estimate the switching for each gate voltage.

The general configuration for the full simulations was designed to sweep the gate voltages while applying a constant source-drain voltage, typically, V_{ds}=1 mV. The voltage applied to each gate was equal in magnitude with opposite polarity, forming a push-pull configuration. The branch currents were extracted by area integration of current density components in the direction of the current (y-direction) from the structure files. The sum of the currents through the branches at each point taken agreed with the total current output by the NEGF solver, supporting our assertion that this calculated current was accurate. This was verified for multiple concentrations and temperatures.

Results and Discussion

With the original goal of simulating the switching of y-branch switches implementing MOS gates, low-voltage switching was demonstrated after confirming that Silvaco Atlas's NEGF solver properly simulated quantum conductance. In the process, however, an energy band profile and charge carrier profile that may be considered ideal for the operation of such devices was found.

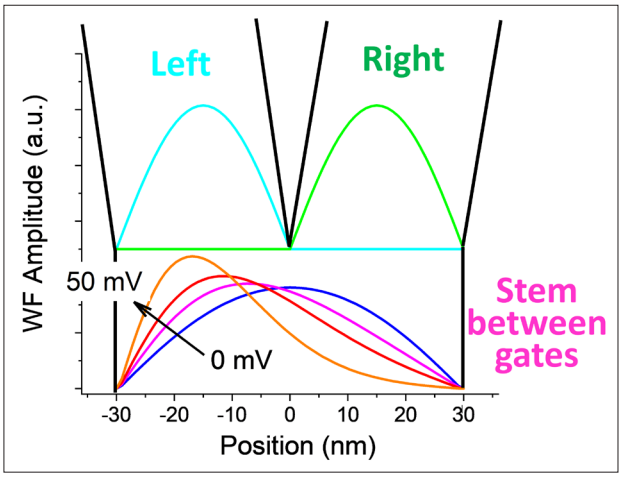

Figure 2: Illustration of wavefunction overlap used for estimates. As a voltage was applied across the gates, the wavefunction in the stem shifts resulting in more overlap with the wavefunction in one branch and less overlap with the wavefunction in the other branch.

Simulation results

As mentioned previously, increasing the concentration at low temperatures to raise the Fermi level should result in the conductance increasing in a step-like fashion. The results of the simulations for V_{ds}=1 mV was shown in Figure 3. The conductance increased by the conductance quantum each time a new subband in the branches began to fill which was illustrated by the band structures along the device length at different doping levels presented in the bottom panel in Figure 3. This confirms the adequate quantum conductance simulation with the chosen technique.

Moving on to the full simulations, the current shifted to one branch while the total current remained relatively constant as the gate voltage was increased. The results of this simulation for the preferred doping concentration can be seen in Figure 4 at 10 K and 77 K. As the figure shows, there was significant switching at gate voltages of just ±10 mV at low temperature. Note these results were obtained for 20 nm long gates. Longer gates will result in the electrons being accelerated to the left or right for a longer duration, thereby increasing the switching effectiveness.

A comparison of our overlap integral predictions to the Silvaco NEGF results can be seen in Figure 5. At 10 K and no gate bias, the structure used has only the first energy level populated everywhere in the device except in the stem very close to the branches. At 77 K thermal electrons just start to populate the fourth energy level in the stem and the second in the branches. It was therefore reasonable to compare the single-subband overlap estimate to the NEGF 10 K result, and the three-subband overlap estimate to the NEGF 77 K result. As the Figure 5. shows, the results were similar to those of the estimates, but the more rigorous calculations demonstrated better switching than the estimates suggested.

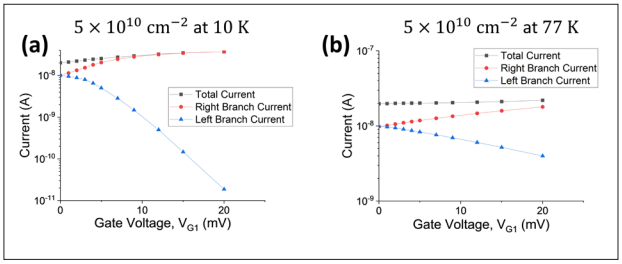

Figure 4: Simulated switching of an YBS with MOS gates using Silvaco Atlas. Significant switching observed at low voltages despite a gate length of only 20 nm. Note that the "Gate Voltage" shown here was the voltage applied to the left gate while a voltage of the same magnitude was applied to the right gate. The differential gate voltage was therefore twice the value shown on the plots. Doping concentration of 5 x 10^{10} cm^{-2} at tempertatures of **(a)** 10 K and **(b)** 77 K.

Proposed ideal band profile

The doping concentration used for switching demonstration was selected as it provided the best current steering without the gate voltage significantly affecting the total current through the device, thus reducing contribution of conventional field effect. Looking at the energy band profile through the stem and branch of the device through x=15.5 nm, z=0 (Figure 6a) it becomes apparent why this was the case. Throughout the length of the gate, only the first level was filled, making it easier to shift the wavefunction and steer the electrons. Then as the electrons approach the junction, the second level begins to populate. The now-populated second level (subband) of the stem was then very well aligned with the ground state in the branches, resulting in a very small energy barrier for the electrons on this second level passing into the first level of the branches. This energy alignment was a result of the thickness of the quantum well being constant throughout the device while the branches were half the width of the stem.

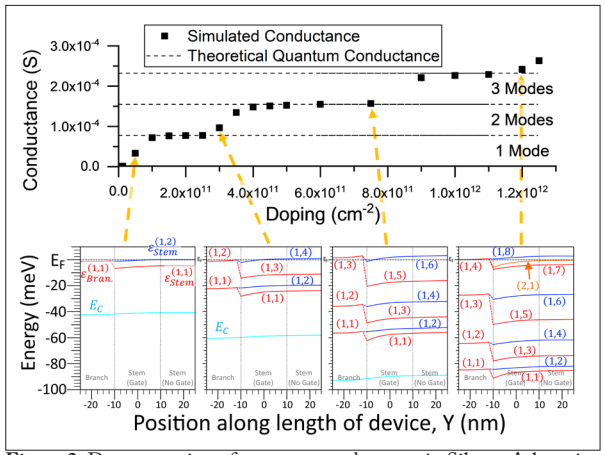

Figure 3: Demonstration of quantum conductance in Silvaco Atlas using the NEGF solver. There was little thermal excitation due to the low temperature, T=10 K. The conductance equals the number of energy levels populated in the branches times the quantum conductance. The lower plots show the energy subbands and conduction band (E_C) relative to the Fermi energy taken through the length of the device for x=15.5 nm and z=0. Each subband in both the branch (left) and stem (center/right) regions of each plot were numbered in terms of confinement (x,z). Notice that the conductance increases by the conductance quantum every time the Fermi level crosses an additional level in the branches.

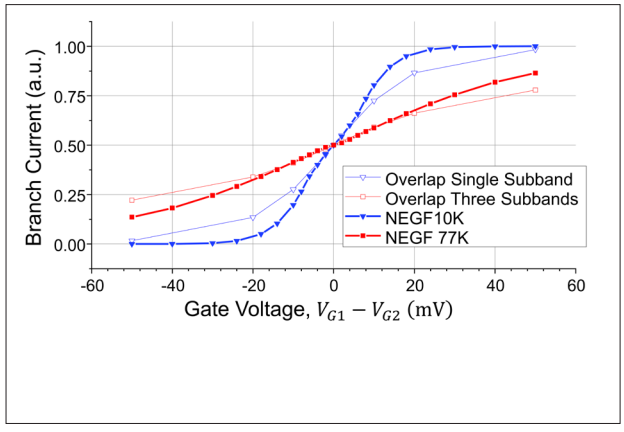

Figure 5: Simulated switching versus switching estimates. The thicker lines represent the Silvaco Atlas NEGF simulation results while the thinner lines represent the wavefunction overlap estimates. It was appropriate to compare the 10 K and 77 K simulations with the single and three-subband results respectively because at 10 K, only the first subband was populated for the doping used, while the forth level in the stem and second level in the branches begin to populate at 77 K.

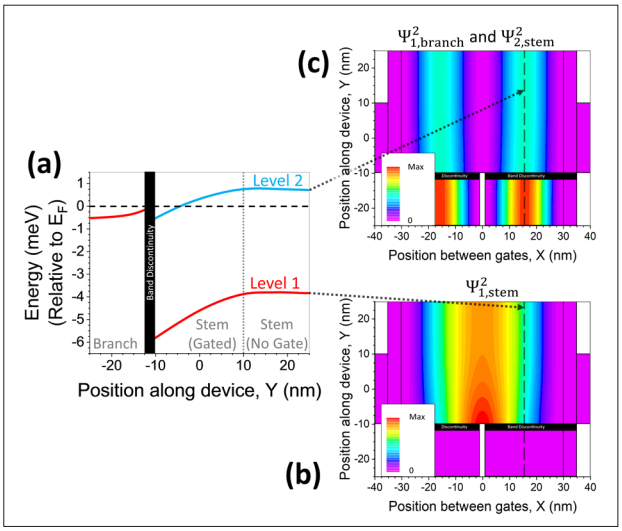

Figure 6: Ideal energy band profile for YBS operation. All slices and cuts taken for z=0. **(a)** Energy band bending at junction for 1.0 x 10^{17} cm^{-3} doping applied to the doping regions (5.0 x 10^{10} cm^{-2}) at 10 K. The excellent alignment between the second level in the stem and first level in the branches results in a very small barrier for electrons. **(b)** $|\Psi|^2$ of the stem first subband containing the majority of the stem electrons, allowing for easy steering. **(c)** $|\Psi|^2$ in the first subband in the branch and the second subband in the stem. Excellent alignment of the wavefunctions results in high transmission.

The branches being half the width of the stem also results in the ground state wavefunctions in the branches having excellent overlap with the wavefunction of the second level in the stem as shown in Figure 6c. This overlap results in reduced reflection. The filling of the branches was also important to maintain a relatively constant current. With a lower concentration, the gate voltage would cause depletion in the "off" branch, which would result in a significant reduction in total current as the FET effect begins to dominate.

Conclusion

Switching in a MOS-gated YBS using Silvaco Atlas codes was demonstrated. The best switching observed without significantly impacting the stability of the total current occurred when the doping concentration resulted in the branch and most of the stem only having their first subband populated with the second subband of the stem partially filling near the junction. With such a band structure, the ground state wavefunction can be easily shifted towards the desired side before transitioning to the second energy level in the stem, which aligns very well with the ground state in the branches, both in terms of energy and spatially. Length limitations make separation of steering and FET effect difficult, but the results suggest that alignment of the subbands at the junction results in better performance. It may be possible to test this by applying different doping to different regions and changing the thickness of the well (energy alignment), and changing the widths of the doped portions of the branches (energy and spatial alignment). The combination should make it possible to determine how much wavefunction overlap and band alignment contribute to the switching performance.

Conflicts of Interest

No conflicts of interest were involved in the study or writing of this paper beyond the funding source disclosed below.

Acknowledgments

This project was supported by the United States Air Force Office of Scientific Research (AFOSR) Contract #: FA9550-19-1-0214, under program manager, Dr. Ken Goretta. The authors would like to thank Professor Vasili Perebeinos for expert help with to Silvaco Atlas and for the computational allocation used to run most of the simulations described in this work.

References

1. Palm T, Thylén L, Nilsson O, Svensson C.1993. Quantum interference devices and field-effect transistors: a switch energy comparison. *J Appl Phys* 74(1): 687-694. https://doi.org/10.1063/1.355231
2. Palm T, Thylén L. 1996. Designing logic functions using an electron waveguide Y-branch switch. *J Appl Phys* 79(10): 8076. https://doi.org/10.1063/1.362362
3. Rahman SFBA, Nakata D, Shiratori Y, Kasai S. 2009. Boolean logic gates utilizing gaas three-branch nanowire junctions controlled by *schottky* wrap gates. *Jpn J Appl Phys* 48(6S): 06FD01. https://doi.org/10.1143/JJAP.48.06FD01
4. Wolpert D, Diduck Q, Ampadu P. 2009. NAND gate design for ballistic deflection transistors. *IEEE Trans Nanotechnol* 10(1): 150-154. https://doi.org/10.1109/tnano.2009.2034962
5. Reitzenstein S, Worschech L, Hartmann P, Forchel A. 2002. Logic AND/NAND gates based on three-terminal ballistic junctions. *Electron Lett* 38(17): 951-953. https://doi.org/10.1049/el:20020652
6. Müller CR, Worschech L, Höpfner P, Höfling S, Forchel A. 2007. Monolithically integrated logic NOR gate based on GaAs/AlGaAs three-terminal junctions. *IEEE Electron Device Lett* 28(10): 859-861. https://doi.org/10.1109/LED.2007.906108
7. Forsberg E. 2004. Reversible logic based on electron waveguide Y-branch switches *Nanotechnology* 15(4): S298. https://doi.org/10.1088/0957-4484/15/4/034
8. Hieke K, Ulfward M. 2000. Nonlinear operation of the Y-branch switch: Ballistic switching mode at room temperature. *Phys Rev B* 62(24): 16727-16730. https://doi.org/10.1103/PhysRevB.62.16727
9. Forsberg E, Hieke K. 2002. Electron waveguide Y-branch switches controlled by Pt/GaAs Schottky gates. *Physica Scripta* 101(1): 158-160. https://doi.org/10.1238/physica.topical.101a00158
10. Seoane N, García-Loureiro AJ, Kalna K, Asenov A. 2007. Impact of intrinsic parameter fluctuations on the performance of HEMTs studied with a 3D parallel drift-diffusion simulator. *Solid State Electron* 51(3): 481-488. https://doi.org/10.1016/J.SSE.2007.01.030
11. Oktyabrsky S, Nishi Y, Koveshnikov S, Wang WE, Goel N, et al. 2010. Materials and technologies for III-V MOSFETs. In: Oktyabrsky S, Ye P (eds) Fundamentals of III-V Semiconductor MOSFETs, Springer, Boston, MA, USA. pp 195-250. https://doi.org/10.1007/978-1-4419-1547-4_8
12. Hinkle CL, Sonnet AM, Vogel EM, McDonnell S, Hughes GJ, et al. 2008. GaAs interfacial self-cleaning by atomic layer deposition. *Appl Phys Lett* 92(7): 071901. https://doi.org/10.1063/1.2883956
13. Xuan Y, Ye PD, Lin HC, Wilk GD. 2006. Minority-carrier characteristics of in GaAs metal-oxide-semiconductor structures using atomic-layer-deposited Al_2O_3 gate dielectric. *Appl Phys Lett* 89(13): 132103.

https://doi.org/10.1063/1.2357566

14. van Wees BJ, van Houten H, Beenakker CWJ, Williamson JG, Kouwenhoven LP, et al. 1988. Quantized conductance of point contacts in a two-dimensional electron gas. *Phys Rev Lett* 60(9): 848-850. https://doi.org/10.1103/PhysRevLett.60.848
15. Landauer R. 2010. Spatial variation of currents and fields due to localized scatterers in metallic conduction. *IBM J Res Dev* 1(3): 223-231. https://doi.org/10.1147/rd.13.0223