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Characteristics Analysis of DMG - SOI MOSFET Using Both High-k and Low-k Dielectrics Materials

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Abstract

Advancement in nanodevice is possible through improving either the nano-device structure with nano engineering techniques or by introducing material-based modification. In this paper, dual material gate silicon-on-insulator (DMG - SOI) metal-oxide-semiconductor field effect transistor (MOSFET) using zirconium dioxide (ZrO_2), a high-k gate dielectric material, is studied for the first time. The device simulated has been carried out on the device performance of nanoscaled DMG - SOI MOSFETs using ZrO_2, a high-k gate dielectric material. To explore the behaviors of the threshold voltage variation and the drain current, a device simulation has been conducted using both low-k and high-k dielectric material. Based on these behaviors, additional research into the transconductance, drain-conductance, and I_{on}/I_{off} ratio for ZrO_2 has been done, and the results have been compared to that of silicon dioxide (SiO_2). High-k dielectric material enables outstanding device performance with the proposed structure when compared to structures using two distinct gate dielectric materials, according to the study. This research paper will be concluded by summarizing the key findings and their implications for the characteristics analysis of nanoscaled DMG - SOI MOSFET in the context of nanotechnology and nanoscience.

Keywords

Dual material gate, Silicon on insulator, Short channel effect, High-k dielectric, Low-k dielectric

Introduction

The first transistor was invented in 1947 [1] and following the invention of the integrated circuit by Jack Kilby in 1958 [2], advances in microelectronics began to improve the performance and increase the circuit complexity to reduce production costs. Such improvement in transistor performance continues to challenge component designers to meet the electronics industry's goals for new requirements for lower-power, smaller, faster, and more reliable integrated circuits. The properties of a MOSFET deteriorate because of the race for downsizing, which has driven device dimensions down to sub-micron levels below 50 nm for improved device performance and higher density integration. However, in the nanoscale regime, several physical limitations known as short channel effects such as drain-induced barrier lowering (DIBL), impact ionization, punch through effect, velocity saturation, etc., limit the down scaling of traditional complementary metal-oxide-semiconductor (CMOS) technology [3-7]. Due to charge-sharing between the source, drain, and channel whenever the channel length is reduced, short-channel effects cause threshold voltage (V_{th}) to roll off. Additionally, off-state leakage current starts to rise because of the sensitivity of DIBL [8-11]. As a result, the many non-traditional CMOS technologies provide researchers with fruitful ways to lessen the downside of the downscaling techniques. Among these novel technologies, SOI nanodevice, particularly FD-

SOI and various SOI nanodevice structures, have gained popularity because of their straightforward manufacturing processes and numerous advantages over CMOS structures in term of device parameter. Many works on SOI - MOSFET are reported so far but for the first time here another novel device model called DMG - SOI MOS (two gate materials are stacked with heterogeneous work function to form the gate electrode) provides a better solution against different short channel effects over conventional CMOS technology [12-16]. Two metals with various work functions are used in the gates material 1(M1) and material 2 (M2) of this structure. Due to a step in the surface-potential profile, this design, as opposed to a single-gate MOS, simultaneously increases transconductance while decreasing SCEs. To ensure that the average electric field beneath the gate is elevated, the DMG construction reduces the peak electric field at the drain end. This increases the device's lifespan, lessens the chance that localized charges may increase drain resistance [17-19], and offers the gate more control over the conductance of the channel, enhancing the gate's transport efficiency. The channel region beneath the material is screened because of the surface potential's step function profile. The gate dielectric thickness is typically reduced as well during this scaling-down procedure to boost gate capacitance. Increased drive current from the increased gate capacitance boosts the device's performance. Unfortunately, it also causes leakage current because of the tunneling phenomena, which increases power consumption and lowers the dependability of the device. Hence, a high-k dielectric material can be utilized as a gate-dielectric instead of traditional SiO_2 to get over this restriction. This can increase gate capacitance without compromising the device dependability related to leakage current. Hafnium dioxide/silicate and ZrO_2/silicate are two materials that have drawn a lot of attention from researchers as high-k dielectric materials to swap out conventional gate dielectric SiO_2. For the first time in this research, the traditional SiO_2 having dielectric constant of 3.9 has been replaced with ZrO_2 as the gate dielectric material in the structure of DMG - SOI nanodevice, which has a maximum dielectric constant of 23. Platinum and titanium have the work function of 4.7 eV and 4.1 eV respectively, have also been employed side by side in this suggested device configuration. The improvement of the drain-induced barrier lowering, and hot carrier impact is the main goal of the proposed work. At the same time, it reveals that the DMG - SOI nanodevice structure performs better when using ZrO_2 as the gate dielectric material in terms of drain current, threshold voltage, transconductance, drain conductance, and I_{on} and I_{off} ratio. As MOSFETs continue to play a crucial role in developing nanoelectronics, research on the design and implementation of DMG - SOI MOSFETs in nanoscaled regime has garnered considerable interest. This analysis will provide significant insights into the potential applications of these materials in nanoscale semiconductor devices.

Experimentation

Device structure and modelling

Figure 1 represents the cross-sectional view of DMG - SOI nanodevice structure having different layers and the following dimensions are in micrometer. ATLAS simulator

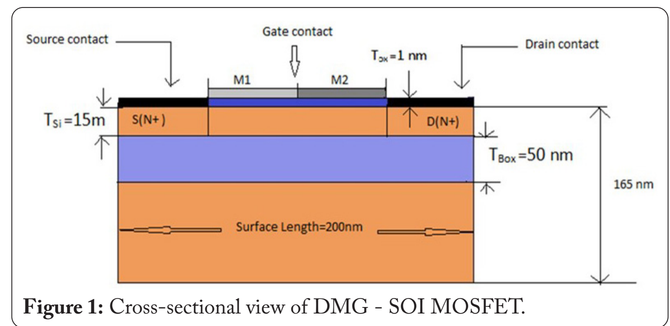

Figure 1: Cross-sectional view of DMG - SOI MOSFET.

is used to simulate nanoscaled DMG - SOI MOSFET (SILVACO). The basic beginning structure is thought to consist of a substantial layer of silicon beneath (the substrate), a comparatively thin layer of SiO_2 on top of the substrate layer, and a silicon thin coating is added on top last (channel). After the basic framework has been put in place, the ATLAS simulator is used to construct the DMG - SOI nanodevice, which is then assembled using oxidation, materials deposition, diffusion, etching, and other processes. The drain current value with respect to gate voltage and the drain current with respect to drain voltage curves, respectively, were used to get the transconductance and the drain conductance value. The simulated structure of a nanoscaled DMG - SOI MOSFET in the ATLAS simulator is depicted in figure 2.

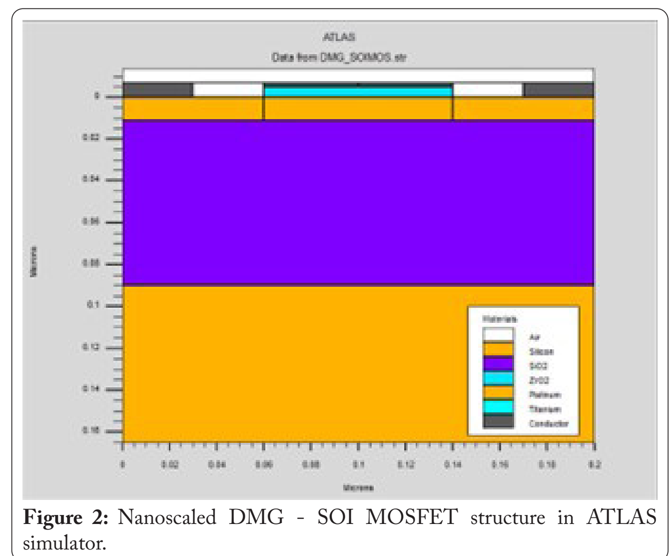

Figure 2: Nanoscaled DMG - SOI MOSFET structure in ATLAS simulator.

The specification of the above structure of DMG - SOI nanodevice is given in table 1. In this work mainly the characteristic of this nonconventional MOS is implemented in ATLAS-simulator (TCAD software) which contain ZrO_2 as high-k gate dielectric material and SiO_2 as low-k gate dielectric material with Materia-1 (Platinum) and Material-2 (Titanium) two different gate material where they have different work function. It is a comparative study with both low-k and high-k gate dielectric materials (SiO_2 and ZrO_2) to study the drain current, drain conductance, transconductance and the ON current and OFF current ratio as well as threshold voltage.

Results and Discussion

Figure 3 illustrates the drain current of a DMG - SOI nanodevice with respect to the drain voltage for both a

Table 1: The device parameters of nanoscaled DMG - SOI MOSFET.

Parameters	Values
Source length and drain length	60 (nm)
Gate length (Lg)	80 (nm)
Channel length (Lch)	80 (nm)
Thickness of gate oxide (TOx)	5 (nm)
Thickness of silicon film (TSi)	11(nm)
Thickness of buried oxide (TBox)	80 (nm)
Thickness of substrate	74 (nm)
Substrate concentration	1 x 10^{17} (cm^{-3})
Source and drain concentration	1 x 10^{21} (cm^{-3})

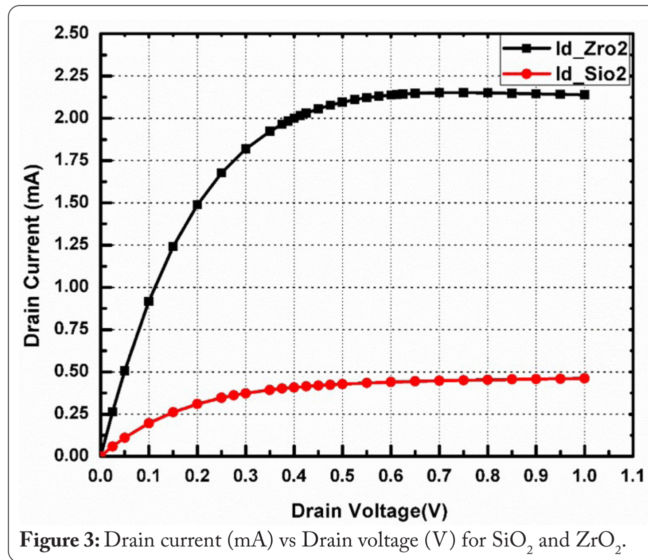

Figure 3: Drain current (mA) vs Drain voltage (V) for SiO_2 and ZrO_2.

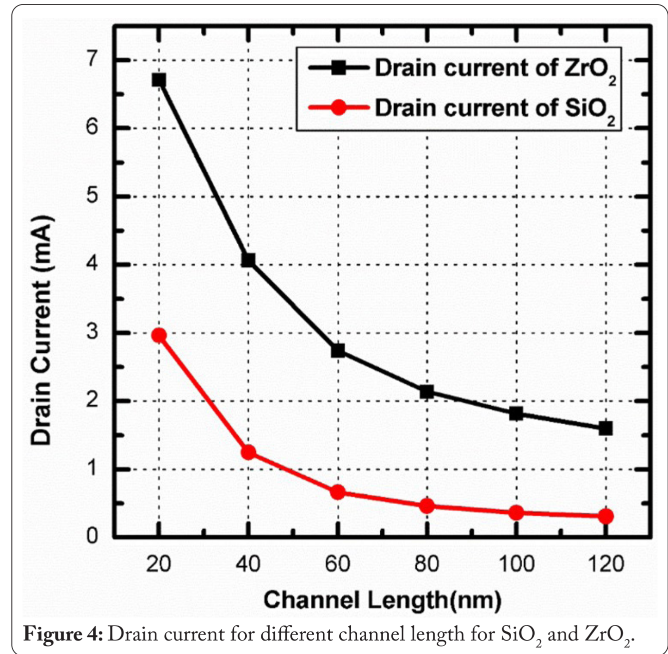

Figure 4: Drain current for different channel length for SiO_2 and ZrO_2.

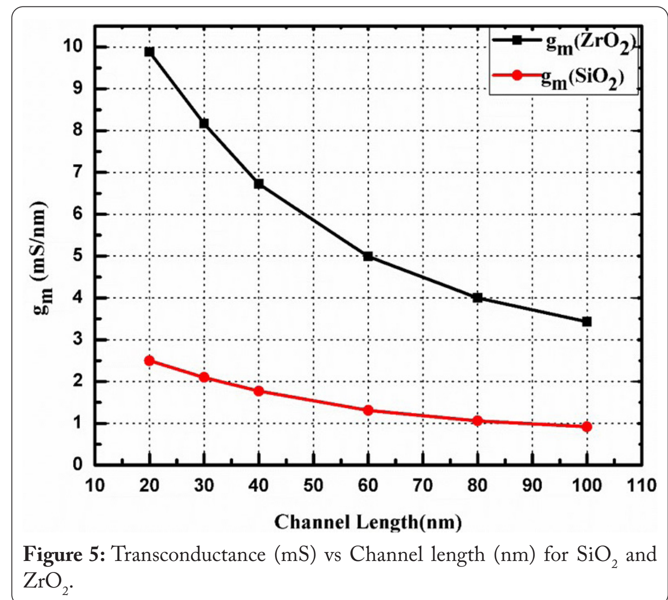

Figure 5: Transconductance (mS) vs Channel length (nm) for SiO_2 and ZrO_2.

high-k gate dielectric material (ZrO_2) and a low-k gate-dielectric material (SiO_2). When the drain voltage rises, we see a higher current for high-k gate dielectric material (ZrO_2) than for low-k gate dielectric material (SiO_2). The outcome demonstrates that anytime low-k gate dielectric material is switched out for high-k material, the amount of drain current rises. By lowering various SCEs like DIBL and the hot carrier effect, the high-k dielectric material improves the efficiency of carrier transport through the channel and lowers the threshold voltage. As a result, large k improves the drain current of the proposed structure in this result.

Figure 4 shows the drain current of nanoscaled DMG - SOI MOSFET for both the high-k material (ZrO_2) and low-k material (SiO_2) with respect to channel length. For ZrO_2 as gate dielectric material we are getting more current than that of SiO_2 as gate dielectric material for different channel length. The result shows that the amount of drain current is reducing continuously whenever the channel length is increasing. The data is extracted from TCAD software and plotted in Origin software for different channel lengths.

Figure 5 represents transconductance (gm) of nanoscaled DMG - SOI MOSFET using ZrO_2 as gate dielectric material and SiO_2 as gate dielectric material with different channel length. For high-k gate dielectric material it provides high transconductance in compared to low-k gate dielectric material with channel length plotted over here. It has been observed that when the channel length being increased, the transconductance value decreases for both the gate dielectric. Here, high-k gate dielectric material offers higher gate insulation capacitance and effective carrier mobility, which provides higher value of the transconductance as compared to the low-k dielectric. The transconductance is measured in between V_{gs} = 1 V and V_{gs} = 0.5 V.

Figure 6 shows drain conductance (gd) of DMG - SOI nanodevice using ZrO_2 as gate dielectric material and SiO_2 as gate dielectric material with different channel length. For high-k gate dielectric material we are getting low transconductance but for low-k gate dielectric material gd is much high with channel length plotted over here. So, the high-k material provides better results as compared to low-k material. The data is extracted from TCAD software and plotted in Origin software for different channel lengths.

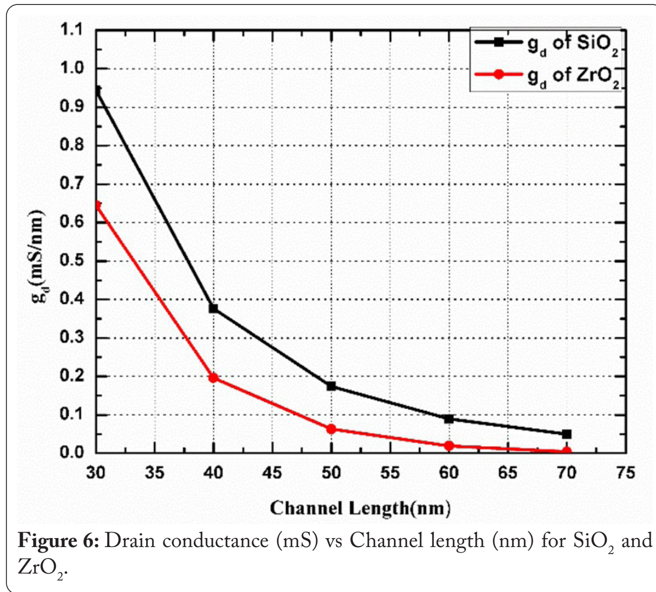

Figure 6: Drain conductance (mS) vs Channel length (nm) for SiO_2 and ZrO_2.

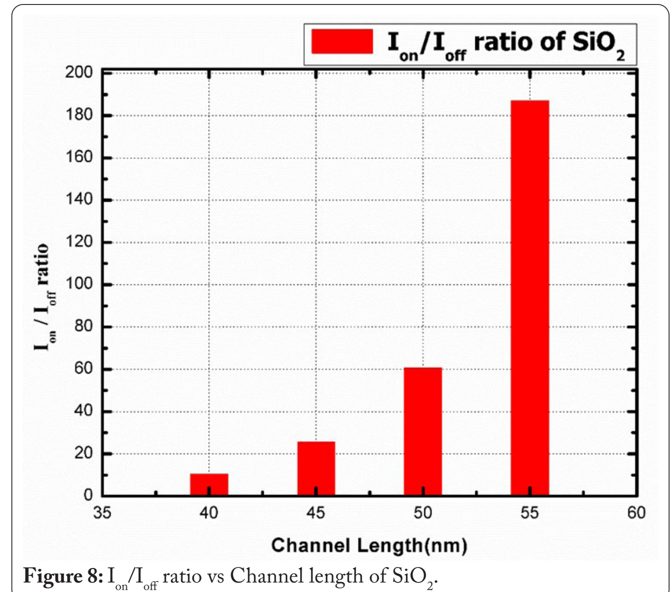

Figure 8: I_{on}/I_{off} ratio vs Channel length of SiO_2.

Figure 7 illustrates threshold voltage (V_{th}) with respect to channel length for both high-k and low-k material of DMG - SOI nanodevice. Here it's clear that the V_{th} high-k of is lower as compared to low-k material as well as the slop of the curve is less. So, the proposed high-k gate material exposing better response than that of the conventional SiO_2 gate dielectric material.

Figure 8 and figure 9 shows I_{on}/I_{off} ratio for different channel length of DMG - SOI nanodevice using SiO_2 and ZrO_2 as gate dielectric material, respectively. Here the high-k material provides much more I_{on}/I_{off} ratio value as compared to low-k material for different channel length plotted over Origin software for different channel length. So, the leakage current is less for the proposed dielectric material (ZrO_2) as compared to SiO_2 used as dielectric material.

Table 2 shows the comparative study of drain current, transconductance, threshold voltage and I_{on}/I_{off} ratio for the channel length of 40 nm for both the high-k as well as low-k material. The table represents the performance of high-k material over low-k material used as gate dielectric. Table 3 also represents the comparative study for 50 nm channel length. From these two tables, in every aspect of device parameter high-k material is superior compared to low-k dielectric material.

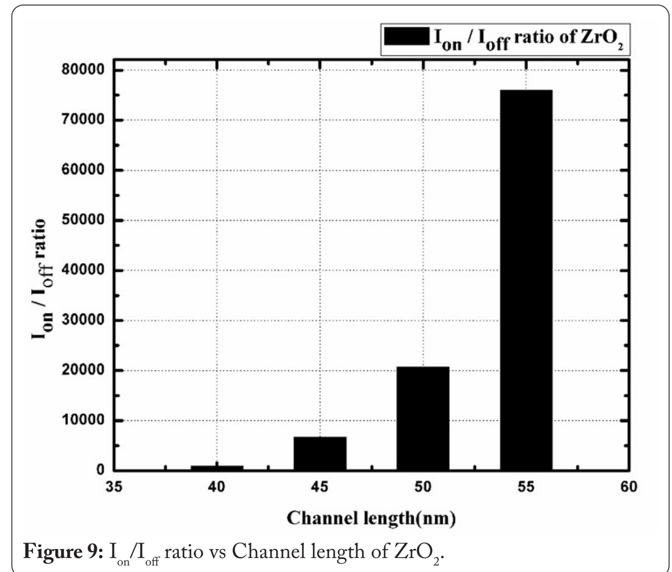

Figure 9: I_{on}/I_{off} ratio vs Channel length of ZrO_2.

Table 2: The simulated results of the proposed structure for different material in the tabulated form (considering the channel length 40 nm).

S. No.	V_{gs} (V)	V_{ds} (V)	Parameter	Material used	Value
1	1	1	Drain current (Id)	SiO_2	1.25 (mA)
				ZrO_2	4.07 (mA)
2	2	0.5 - 1.0	Transconductance (gm)	SiO_2	1.77 (mS/nm)
				ZrO_2	6.728 (mS/nm)
3	1	0.65 - 1.0	Drain conductance (gd)	SiO_2	0.376 (mS/nm)
				ZrO_2	0.196 (mS/nm)
4	2	1	Threshold voltage (V_{th})	SiO_2	0.30 (V)
				ZrO_2	0.25 (V)
5	2	1	I_{on}/I_{off} ratio	SiO_2	10.4
				ZrO_2	905

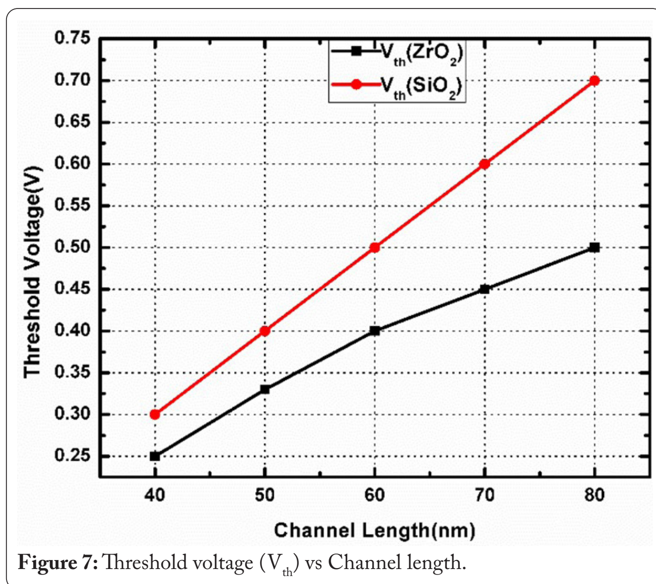

Figure 7: Threshold voltage (V_{th}) vs Channel length.

Table 3: The simulated results of the proposed structure for different material in the tabulated form (considering the channel length 50 nm).

S. No.	V_{gs} (V)	V_{ds} (V)	Parameter	Material used	Value
1	1	1	Drain current (Id)	SiO_2	0.866 (mA)
				ZrO_2	3.20 (mA)
2	2	0.5 - 1.0	Transconductance (gm)	SiO_2	1.0 (mS/nm)
				ZrO_2	5.8 (mS/nm)
3	1	0.65 - 1.0	Drain conductance (gd)	SiO_2	0.174 (mS/nm)
				ZrO_2	0.0629 (mS/nm)
4	2	1	Threshold voltage (V_{th})	SiO_2	0.4 (V)
				ZrO_2	0.33 (V)
5	2	1	I_{on}/I_{off} ratio	SiO_2	60.7
				ZrO_2	20700

Conclusion

In this work, the simulation in ATLAS simulator of DMG - SOI nanodevice structure with both low-k (SiO_2) and high-k (ZrO_2) gate dielectric material has been carried out the investigation for the different parameters of the device such as drain current, transconductance, drain conductance and I_{on}/I_{off} ratio and threshold voltage. In this work, ZrO_2 has been used in place of SiO_2 as a gate dielectric material to provide high value of gate capacitance and the effective carrier mobility to the proposed device structure. The use of ZrO_2 as a high-k dielectric decreases various SCE, s effects like DIBL, hot electron effects, etc., and it gives better results in terms of all the parameters like drain current, transconductance, drain conductance and I_{on}/I_{off} ratio and threshold voltage, etc. Therefore, it can be concluded that the ZrO_2 as a high-k gate dielectric material provides better performance for the CMOS circuit application in the nano-regime compared to its low-k gate dielectric.

Acknowledgments

None

Conflict of Interest

None

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