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Research Article

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Analysis of Geometric Parameter Variation Effect on Electrostatic Characteristics of 3D Double Gate Junctionless Transistor

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Abstract

In this paper we have investigated the effect of device geometry parameters on junctionless transistor's (JLTs) electrostatic characteristics. Emphasis is given on variation in gate length, gate oxide thickness and channel doping concentration to understand the scalability of JLT. Critical properties like threshold voltage, subthreshold swing, transconductance are evaluated for down scaled JLT structures to understand the optimization of device parameters. Low gate oxide thickness and apposite doping concentration is required to fully deplete the channel and maintain high current, respectively.

Keywords

Junctionless transistor, Short channel effects, Double gate, Transconductance

Introduction

Incessant development in complementary metal-oxide-semiconductor technology has become essential to meet design and implementation issues of the present-day low power, high speed, and high-performance requirements. Devices are down scaled to exhibit improved functionality, high packing density, low power dissipation, and high speed. In the process of extreme scaling of transistor dimensions, conventional metal-oxide-semiconductor (MOS) devices are facing different limitations. As a response of scaling problems, several novel structures and new material are introduced to fulfill the requirements of present VLSI era. To diminish the short channel effects and achieve the goals of modern era researchers have invested their knowledge, infrastructure, and precious time to develop novel devices and new technology. Short channel effects (SCEs) are the main drawback of devices in nanometer regime [1]. Emerging novel structures like Fin-field effect transistors [2-5], silicon-on-insulator [6-9], tunnel field effect transistor [10-12], carbon nanotube field effect transistor [13-15], spin based device [16-18], ferromagnetic logics [19-21], junctionless field effect transistor [22-24] were introduced and investigated to alleviate the challenges of conventional metal-oxide-semiconductor field effect transistor (MOSFETs). Development of such devices may take microelectronics industry to new heights.

As an alternative to conventional devices with junctions, a junction-free exceptional novel structure architecture was firstly proposed in 2009 [22] and later fabricated in 2010 [23]. Though the 'JLT' has a virtue of easy fabrication and eliminates the problems of impurity diffusion and requirement of sharp junction, aggressive scaling study of JLT is very essential to have a complete understanding. In this study, the basic overview of JLT in terms of device structure, operating principle and physics is discussed. Though research on JLTs have proved its technological advantages over conventional inversion mode MOSFETs, no devices are fully free from challenges in extreme scaling conditions. In the paper, a JLT

with double gated structure of 20 nm gate length is considered for investigation. Gate all around transistors provide better electrostatics than fin-field effect transistors or double gates and allow for some additional gate length scaling. So, it may become a key to migrate to 5 nm regime. But gate all around fabrication faces critical challenging in making the patterns, gates, nanowires, and interconnects, which make it not much feasible or not even cost effective. Due to this reason, we chose more easily fabricate-able double gate structure for the study. The emphasis is given on the variation of JLT structural design parameters and electrostatic characteristics variation with the change in JLT parameters.

To assess the challenges to be faced in scaling of JLT device structure, tunability of device parameter is tested in this study. When a new semiconductor device-JLT was introduced, the emphasis was usually given on their device characteristics. Section 2 presents the details of proposed device structure and a computer platform-technology computer aided design (TCAD) Tool used for the study. The simulation models used in TCAD tools are also briefly discussed in the section 2. Further, simulation result is calibrated with an experimental result available for JLT. Section 3 contains the analysis of the electrostatic characteristics of JLT with variable device structure parameter. Subsection 3.1 explains the gate length down scaling effect of JLT on its electrostatic integrity. Channel body thickness and channel doping concentration variation is studied in subsection 3.2 and 3.3, respectively. Gate oxide variation effect on JLT characteristics is explained in 3.4. Lastly, summary of the work is presented in section 4.

Experimentation

Device design environment

Synopsys TCAD tool is used to simulate and analyse the JLT devices for our study. Simulation work comprises of three parts: JLT structure preparation, device physics simulation through different numerical methods and data extraction. 3D JLT structures are built on Synopsys structure editor3D, Device Simulator (Sdevice) used for device physics simulation. Data extractions for output visualization are performed through Svisual, Inspect. Device mashing is performed by mashing engine called from interface available in the structure editor3D. Different physics models are included in Sdevice to simulate for specific conditions and parameter values. Drift-diffusion model and High Field Saturation model are used for current transport and mobility, respectively. Further mobility degradation model – Enormal and recombination models of Auger, SRH and avalanche are also incorporated to bring more effectiveness.

A simple double gate JLT and gate length is considered as 20 nm throughout our investigation unless it is mentioned. 3D structure prepared in Synopsys 3D device structure editor is shown in figure 1. Width and thickness of the silicon wire is 12 nm and 10 nm, respectively. The silicon wire is doped with arsenic of 1.5 x 10^{19} cm^{-3} concentration uniformly. Silicon dioxide (SiO_2) of 1 nm thickness is used as a gate oxide for all the devices. Polysilicon gate with work-function 4.23 eV is used at the gate metal. The simulator is calibrated with the

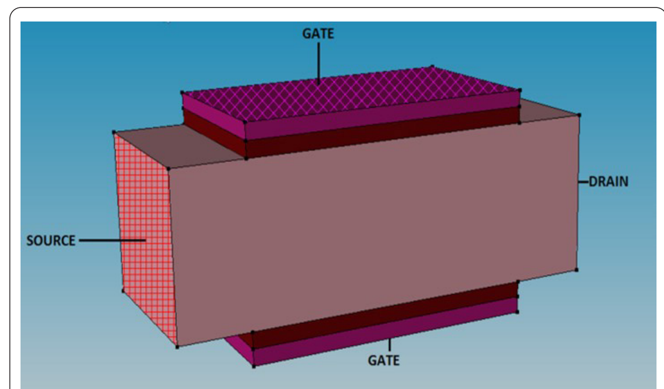

Figure 1: 3D double gated JLT [25].

experimental values available for JLT of 1 μm long gate and 30 nm width [23]. The calibrated result of the simulator for p-type and n-type JLT is shown in figure 2.

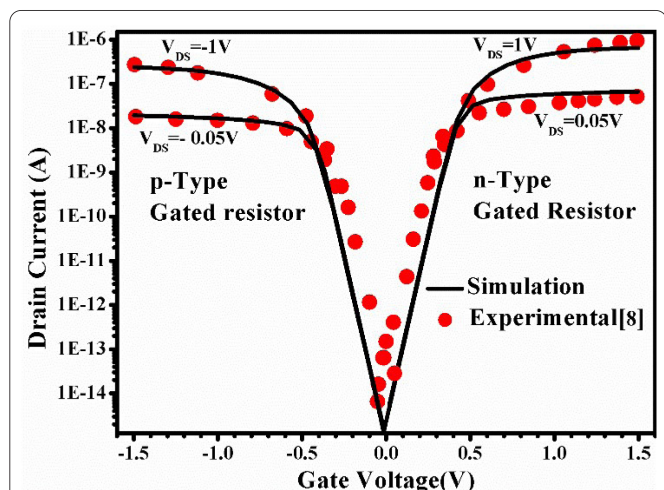

Figure 2: Calibration of the simulator against the experimental data available for JLT of 1 μm gate length and 30 nm width.

Results and Discussion

Effect of geometric parameter variation in proposed device

To understand the JLT characteristics variability and dependency with different geometric parameter a synchronized study is required. In this section, we have studied the characteristics and performance of JLT for variable geometric parameters. At a time one parameter is scaled and rests are kept on their proposed value.

Gate length variation of JLT

To see the scalability of the double gate JLT, the gate length is varied from 40 nm to 10 nm. The transfer characteristic of the JLT with different gate length is given in figure 3. Increase in the drain current can be seen with the decrease in gate length. Decrement in threshold voltage also observed with gate length increase. Further, subthreshold swing has increased with the gate length down scaling. Subthreshold swing is 63.8 mV/decade for 40 nm gate length which is very near to the fundamental value 60 mV/decade. But the SS performance deteriorates to 260 mV/decade for 10 nm gate length. In 20 nm gate length, the JLT has 77.7 mV/decade subthreshold swing.

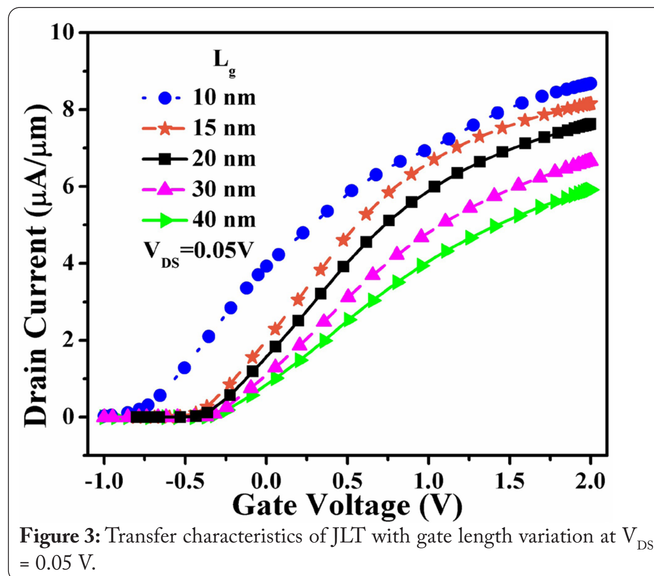

Figure 3: Transfer characteristics of JLT with gate length variation at V_{DS} = 0.05 V.

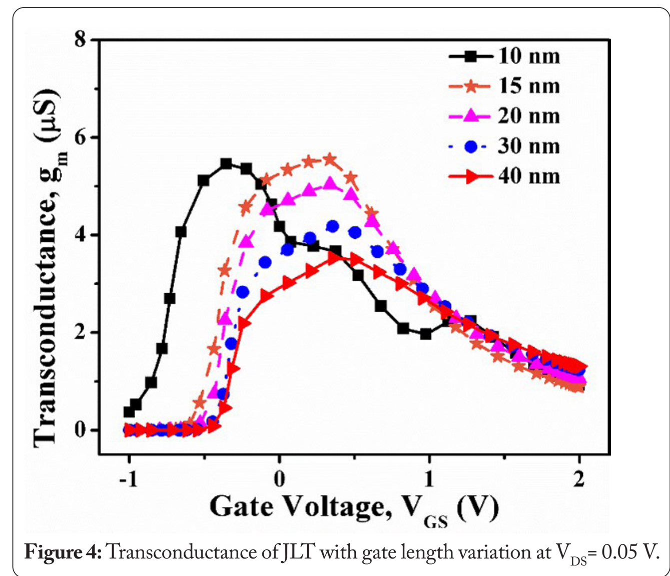

Figure 4: Transconductance of JLT with gate length variation at V_{DS}= 0.05 V.

The detail comparison of threshold voltage, subthreshold swing, and 'on' current for different gate length with V_{DS} = 0.05 V is mentioned in table 1. To make a depletion in n substrate a negative voltage (or $V_{GS} < V_{FB}$) is required to apply at gate. Decrease in gate length in a short channel junctionless device will increase the centre potential of channel. As because in short channel device source and drain are very near, only one minimum channel potential point is present in channel. So, further decrease in the gate length will push the minimum point to higher potential. Due to decrement in barrier height, threshold voltage also decreases. As a result, less amount of gate voltage will be required to turn on the device. On the other hand, more negative voltage is required to make full depletion in channel. This phenomenon is called threshold voltage roll-off. Threshold voltage roll-off also been observed in JLT like IM-MOSFETs. Though current has increased in JLT with shorter gate length, threshold voltage has decreased, and subthreshold swing has deteriorated. The transconductance characteristics of JLT in figure 4 show that transconductance increases with the down scaling of the device. So, analogue characteristics of lower gate length JLT will be better.

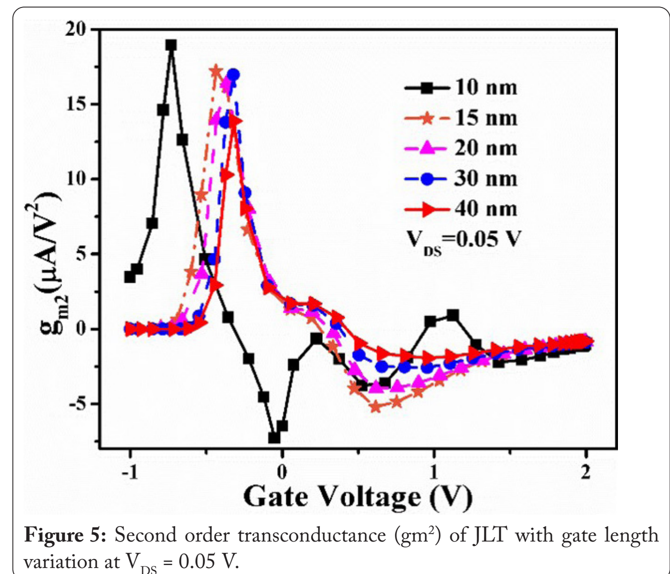

Figure 5: Second order transconductance (gm²) of JLT with gate length variation at V_{DS} = 0.05 V.

Table 1: Performance of JLT for different gate lengths.

Gate length (L_g)	Threshold voltage (V_{th})	Subthreshold swing (mV/decade)	'On' current at V_{GS} = 2 V
40 nm	-0.214 V	63.8	5.91 μA
30 nm	-0.223 V	66.8	6.66 μA
20 nm	-0.304 V	77.7	7.62 μA
15 nm	-0.359 V	101	8.16 μA
10 nm	-0.738 V	260	8.67 μA

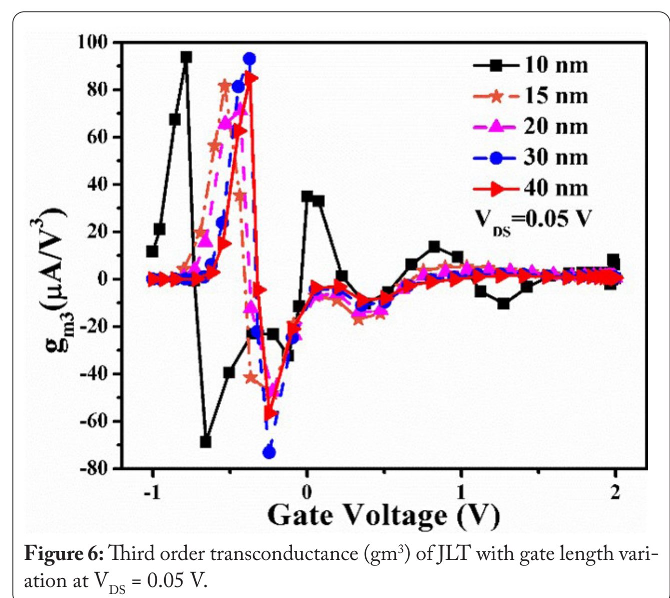

Figure 6: Third order transconductance (gm³) of JLT with gate length variation at V_{DS} = 0.05 V.

Second order transconductance (gm²) of JLT in figure 5 shows that JLT with higher gate length has lower gm² peak and thus it gives better linearity as compared to lower gate length. Third order transconductance (gm³) of JLT for different gate lengths in figure 6 are similar. In both the characteristics the peaks occur at different values of gate voltage due to their different threshold voltages. Figure 7 shows the transconductance generation factor (TGF, gm/ID) as a function of gate voltage for different gate length of JLT. TGF gives the measure of the effectiveness of generating

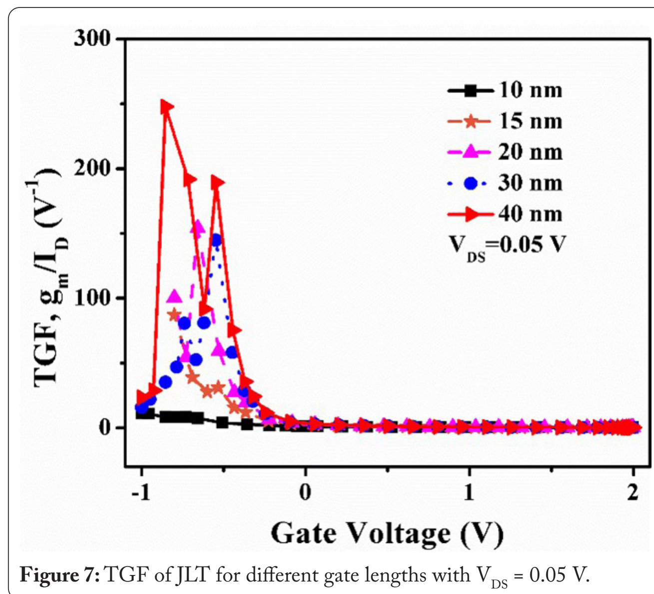

Figure 7: TGF of JLT for different gate lengths with V_{DS} = 0.05 V.

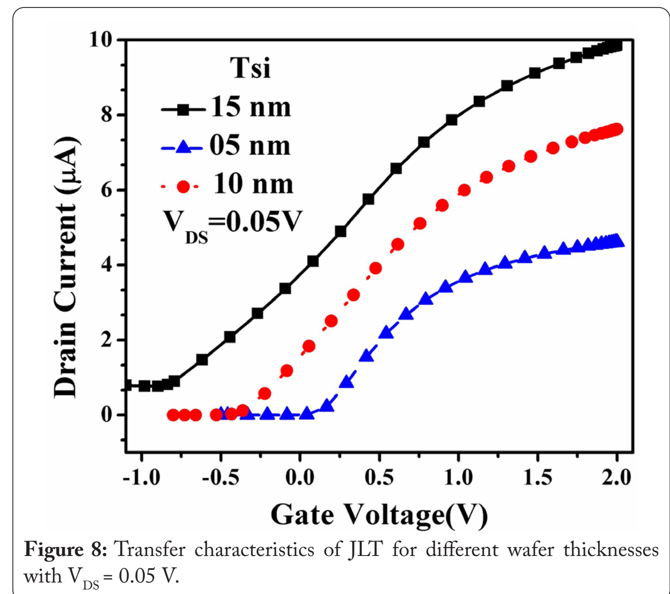

Figure 8: Transfer characteristics of JLT for different wafer thicknesses with V_{DS} = 0.05 V.

conductance. TGF at subthreshold region should be high. TGF decreases with the decrease in gate length of JLT. Above threshold the TGF is constant in JLT for all the gate lengths. Though transconductance (gm) is higher for lower gate length, it has higher drain current (ID). So, decrease in gate length decreases TGF (gm/ID) due to high 'on' current. Decrease in gate length of JLT make current less effective to achieve higher transconductance.

Channel body thickness variation of JLT

The wafer or body thickness of JLT is another critical design parameter. As the JLT conducts through the bulk or body, the whole body should be depleted to turn off the device. So, thickness of the body plays a crucial role in this case. In case of double gate, the thickness should be such that the depletion from both sides meet each other to turn off the device. So, a thin layer body is always desired in such case. But preparation of very thin uniformly doped silicon layer is very difficult and has a need of advance process flow. Due to this, the thickness scalability for double gate JLT is very important to understand the maximum possible thickness of the device structure.

Keeping gate length (20 nm), oxide thickness (1 nm), silicon nanowire/body width (12 nm), and channel doping concentration (1.5 x 10^{19} cm^{-3}) constant, the nanowire/body thickness is varied from 5 nm to 15 nm. Figure 8 shows the drain current vs gate voltage for JLT with silicon body thickness 5 nm, 10 nm, and 15 nm. Though JLT with high silicon body thickness have high drain current, they require high negative gate voltage to turn off the device. So, threshold voltage moves toward negative in case of wider silicon body. Threshold voltage is found to be 0.134 V and -0.304 V for silicon body thickness of 5 nm and 10 nm, respectively. Subthreshold swing is found to be 64 mV/decade and 77.7 mV/decade for silicon body thickness of 5 nm and 10 nm, respectively, whereas JLT with silicon body thickness 15 nm has not turned off.

The electron density in silicon body for gate voltage -1.5 V is shown in figure 9 for JLT with silicon body thickness 5 nm, 10 nm, and 15 nm. Electron density in figure 9a and figure 9b show that JLT with silicon body thickness 5 nm and 10 nm are fully depleted at gate voltage -1.5 V. But JLT with silicon body thickness 15 nm only have partially depleted body and channel between source and drain still exists (Figure 9c). So, the body thickness is too high to deplete by double gate of JLT.

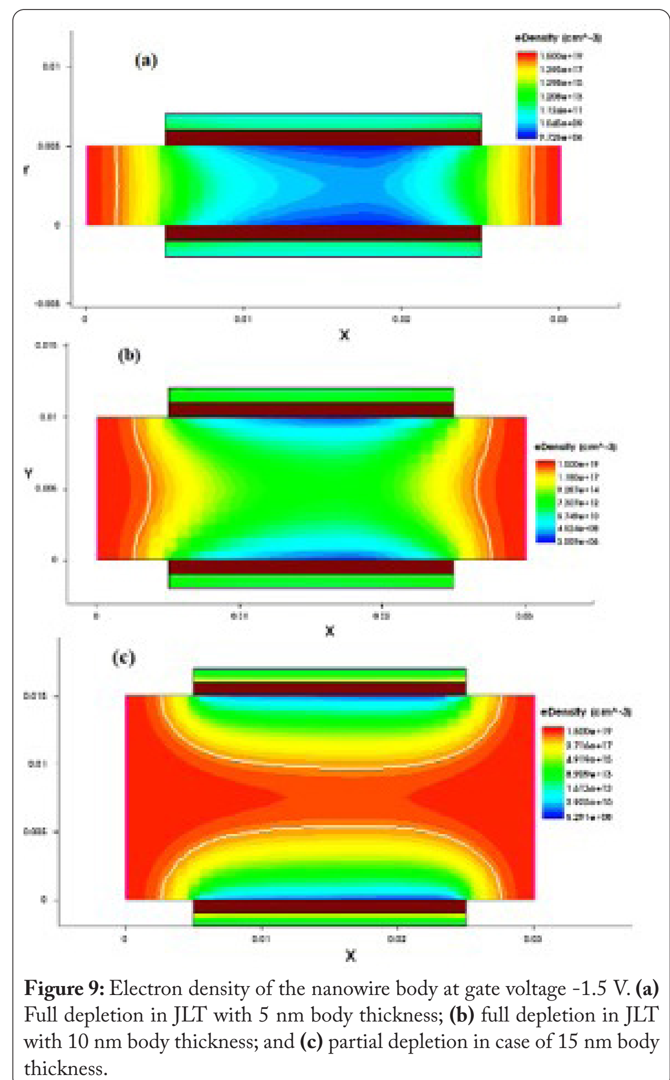

Figure 9: Electron density of the nanowire body at gate voltage -1.5 V. **(a)** Full depletion in JLT with 5 nm body thickness; **(b)** full depletion in JLT with 10 nm body thickness; and **(c)** partial depletion in case of 15 nm body thickness.

Channel doping variation of JLT

Channel doping is another important parameter for any MOS device design. In JLT a uniformly doped silicon nanowire is required. Thin layer body with heavy doping is also has problem of random dopant fluctuation. The ID-VG characteristics of proposed JLT structure with different channel doping are shown in figure 10. As low doped body is easier to deplete, JLT with low doping concentration has more positive threshold voltage. But JLT with lightly doped body gives very less current. As proposed double gate JLT is using a thin silicon body, a high doping is required to achieve enough current. Subthreshold swing, threshold voltage and on-current details for different channel doping concentration in JLT are given in table 2.

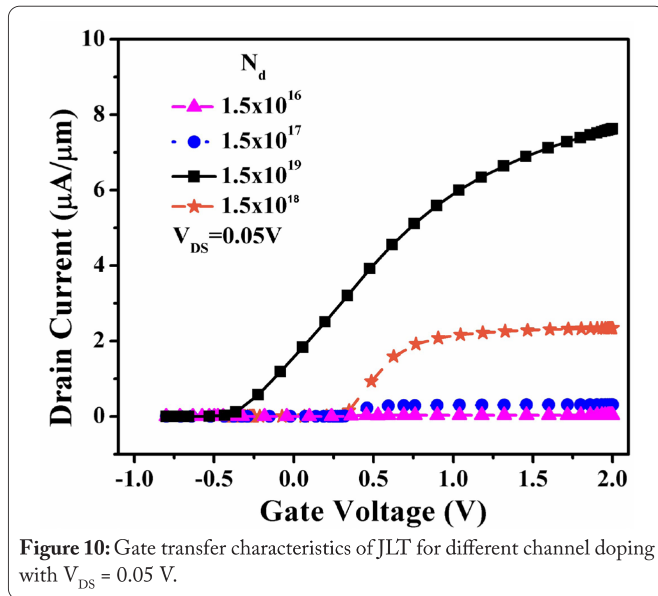

Figure 10: Gate transfer characteristics of JLT for different channel doping with V_{DS} = 0.05 V.

Table 2: Performance comparison of JLT with different channel doping concentrations.

Channel doping (N_D)	Threshold voltage (V_{th})	Subthreshold swing (mV/decade)	'On' current at V_{GS} = 2 V
1.5 x 10^{19} cm^{-3}	-0.304 V	77.7	7.62 μA
1.5 x 10^{18} cm^{-3}	0.289 V	73	2.34 μA
1.5 x 10^{17} cm^{-3}	0.309 V	72.9	0.31 μA
1.5 x 10^{16} cm^{-3}	0.333 V	71.2	0.032 μA

Gate oxide thickness variation of JLT

The gate oxide thickness is very important part of a MOS operation. Dielectric constant (k) of oxide and oxide thickness controls the MOS capacitance. Thin oxide layer will increase the gate capacitance and control of gate over the channel will be stronger. The channel will be easily depleted in less negative gate voltage in JLT with thin gate oxide. To analyze the effect of gate oxide thickness on n-channel double gate JLT electrical characteristics, the JLT structure is simulated for different gate oxide (SiO_2) thickness. Figure 11 shows JLT transfer characteristics for different gate oxide thickness. Table 3 explains the performance of JLT for different gate oxide thickness. JLT with 1 nm gate oxide achieves better subthreshold swing and threshold voltage as compared to other higher gate oxide thickness. 'On' current also high in case of JLT with 1 nm gate oxide, due to its high gate capacitance. A suitable gate oxide thickness is to be chosen to restrict leakage current through the thin gate insulator.

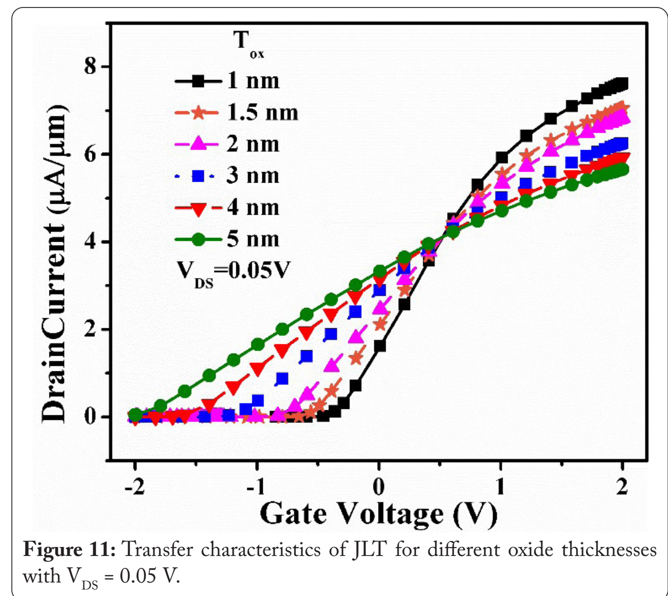

Figure 11: Transfer characteristics of JLT for different oxide thicknesses with V_{DS} = 0.05 V.

Table 3: Performance comparison of JLT for different gate oxide thicknesses.

Gate oxide thickness (T_{ox})	Threshold voltage (V_{th})	Subthreshold swing (mV/decade)	'On' current at V_{GS} = 2 V
5 nm	-1.918 V	270	5.66 μA
4 nm	-1.522 V	133	5.93 μA
3 nm	-1.130 V	110	6.26 μA
2 nm	-0.736 V	95	6.84 μA
1.5 nm	-0.518 V	86.5	7.06 μA
1 nm	-0.304 V	77.7	7.62 μA

Conclusion

Though JLTs are more immune to SCEs as compared to conventional MOSFETs, they are not fully free from SCEs. Gate length variation analysis of JLT shows that JLT performance is deteriorated due to down scaling of the physical gate length. In this paper investigation is performed to understand the device working and effect of geometric design parameter variation on the device characteristics. A thin layer body is required to guarantee the full depletion and full control of gate over channel. Less negative voltage in gate is required for full depletion of channel with low doping concentration. Adequate high doping in ultra-thin channel is required to ensure a good amount of on current. To increase the gate, control a thin gate oxide layer is needed.

Acknowledgments

None.

Conflict of Interest

There are no known conflicts of interest in person or financial..

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