Nano World Journal

https://doi.org/10.17756/nwj.2023-s5-005

Research Article

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A 3D TCAD Model of a Non-aligned Double Gate Symmetrical Junction FET in Nanoscale Regime

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Received: October 11, 2023
Accepted: December 18, 2023
Published: December 21, 2023

Citation: Naik BV, Sinha AK. 2023. A 3D TCAD Model of a Non-aligned Double Gate Symmetrical Junction FET in Nanoscale Regime. *NanoWorld J* 9(S5): S23-S28.

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Abstract

This paper presents result from TCAD simulation of a proposed three-dimensional (3D) non-aligned double-gate n-channel field effect transistor (NADGNFET device). The device has a junction and symmetrical structure with 50% non-alignment in gate placement and 40 nm channel length, giving improved results in various figures of merit used for calibrating nano devices. The device uses a high-k spacer of hafnium oxide (HfO_2) with dielectric constant of 24 placed under the polysilicon forming double gates on the two sides of the NADGNFET device. The device parameters extracted from input and output characteristics simulation were, threshold voltage (V_{TH}), small-signal transconductance (g_m), output conductance (g_{ds}), OFF current (I_{OFF}) and ON current (I_{ON}), total gate capacitance (C_{GG}). Also, various analog figure of merit parameters like subthreshold swing (SS), drain induced barrier lowering, and intrinsic gain (A_{VO}) were measured. The radio frequency (RF) figure of merit parameters like, cut-off frequency (f_T), transconductance generation factor (TGF), and transconductance frequency product (TFP), gain frequency product (GFP), gain transconductance frequency product (GTFP), along with linearity figure of merit like, intercepted input power-3 (IIP3) and intercepted intermodulation current-3 (IMD3), were plotted and measured. The simulation result shows the device achieved a good performance in various figures of merit when compared to the past works.

Keywords

Double gate MOSFET, Figure of merit, Nano device, I_{ON} and I_{OFF} currents, Linearity

Introduction

Implementing a complementary metal oxide semiconductor (CMOS) circuit with metal oxide semiconductor field effect transistors (MOSFET) at sub-100 nm regime is becoming extremely difficult. The device model faces various challenges like short channel effects (SCEs) and transport degradation in mobility. The main aim of the researchers is to reduce the SCEs with the reducing dimensions of a conventional MOSFET. The multi-gate transistors having a double gate (DG), triple gate (TG), gate all around (GAA), reported to have reduced the short channel effects [1]. Also, with increasing frequency in the communication band to fast transmit the data by having least error or without error is the next challenge. Some causes of these errors are signal distortion which occurs at nano scale in the devices [2]. These errors can be rectified with improved signal to noise ratio in CMOS circuits giving less inter-modulation distortion. The semiconductor materials are chosen by their conductivity, and many different compounds are available for transistors out of which silicon is mostly preferred [3], therefore, increased drive current and small signal transconductance are the

preferred requirement. In the single gate sub-100 nm device channel, the leakage current increases due to generation of hot electrons because the source side electric field is low which reduces the device durability, [4]. The SCEs have become significant as device dimensions have downsized and chip implementation density had also increased, requiring the new device design to meet the challenges. To overcome SCEs, multi-gate MOSFETs, the GAA MOSFET has found to be highly efficient. The GAA MOSFETs has better channel management, continue to increase carriers, and improve electrical properties at shorter gate lengths and thinner oxide layers [4]. The design requires reduced drain side current because it lowers the leakage current. Whereas the electric field in a single gate MOSFET is very low near the source side and very high near the drain end. This is due to the injection of hot electrons between the gate and drain, which reduces the device performance and its life. The DG MOSFETs with gate stack configurations have a thicker oxide layer, which decrease gate leakage current and improves electrostatic integrity without requiring a high channel doping.

In this paper, the NADGNFET [5], device behavior is being analyzed with 3D structure using HfO_2 as gate oxide material. Simulation results are presented to show the current-voltage characteristics in sub-100 nm regime through measurement curves. A systematic investigation on the performance by the polysilicon gate-based DG-MOSFET along with non-aligned architecture is also presented. This paper is arranged as follows: Section II presents 3D structure of the NADGNFET device. Also shows various measurements along with the extracted value of analog figure of merit (FOM). Section III presents RF and linearity figure of merit given by the proposed device. Finally, the conclusions are drawn in the Section IV.

Experimentation

Proposed 3D model of a NADGFET device

Figure 1 shows the 3D structure of a NADGNFET device along with various region and dimension. The device length is 90 nm, and width (thickness) is 15 nm, and height is 30 nm, the dimensions are chosen according to the recent trend. The percentage of non-alignment chosen for this device is 50%, i.e., percentage in gate overlap with the source and drain side [5]. A HfO_2 spacer of 5 nm width and 2.5 nm thickness is given, and the polysilicon gate with HfO_2 is used as gate oxide with 1 nm thickness. The electrodes make contact from the outside of the device. The DG is applied to the same gate voltage to turn on the device by inverting the channel. At the source and drain region, a uniform doped junction is used. Source and drain are doped with 1 x 10^{18} cm^{-3} concentration of phosphorous, the channel is doped of 1 x 10^{12} cm^{-3} concentration of boron. The device electric field is applied at the two sides of the gate symmetrically placed in vertical position. In general, when the longitudinal electric field component of the MOS device increases, this decreases the channel length because of extension of depletion layer into the channel region, making surface mobility much field-dependent, however for the present NADGNFET device because of two gate overlaps at the source/drain region, this effect is less dominant. The test using simulation for the proposed device is completed using the 3D-Sentaurus device simulator. All design parameters and supply voltage are chosen according to the International Road map for Semiconductors [6], in present simulation.

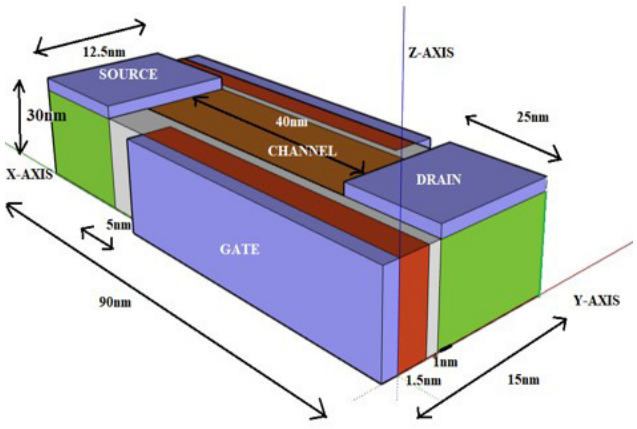


Figure 1: A 3D view of structure showing the proposed NADGNFET device. The green color represents doped n^+ region, red color represents the polysilicon layer, white color represents the HfO_2 as gate oxide, brown color represents p-layer, and blue color represents metal contact.

Analog FOM

Figure 2 and figure 3 shows the characteristic curves of the proposed device, the extracted value of I_{ON}, and I_{OFF} current, were 1.465 mA, and 6.87 pA, at 1 V drain to source voltage, respectively. Depending on the application, the leakage current can be controlled by properly selecting the threshold voltage for the NADGNFET device. It can be observed I_{ON}/I_{OFF} = 2.1 x 10^8, which is best suitable in circuit applications. The device threshold voltage (V_{TH}) is extracted to be 3.85 V, suitable in low power applications. Figure 3 shows the output characteristics, giving average lambda (λ) ≈ 0.8 V^{-1}. Figure 2 and figure 3 preserves the MOSFET characteristic curves without any deviation.

The transconductance (g_m) is an important FOM that describes the device's behavior based on the small change in the drain current [7]. The g_m gives the efficiency at which the device converts gate voltage into a drain current is given by equation 1.

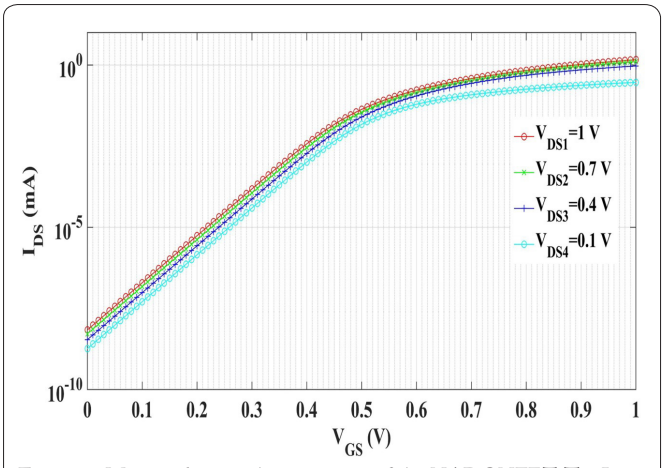


Figure 2: Measured input characteristics of the NADGNFET. The I_{DS} is drain to source current.

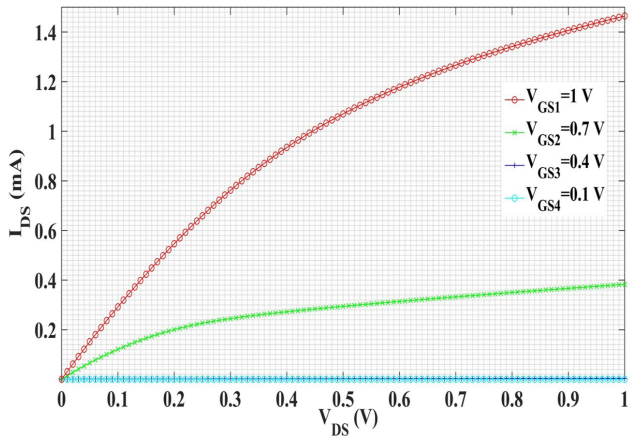


Figure 3: Measured output characteristic of the NADGNFET device.

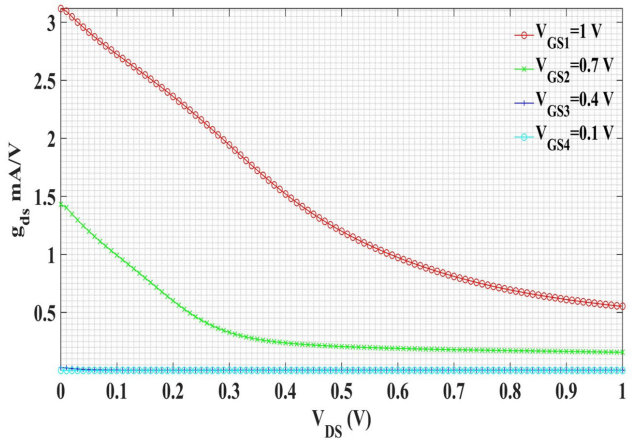


Figure 5: The output conductance plot of the NADGNFET device.

$$g_m = \left.\frac{\partial I_{DS}}{\partial V_{GS}}\right|_{V_{DS}=k} \quad (1)$$

In equation 1, the g_m is measured for HfO_2 based poly-silicon gate NADGNFET device as shown in figure 4, it is the large value considering the requirement for device gain in operational amplifiers and functional transconductance amplifiers. The g_m values initially affect the AC gain, bandwidth, the offset occurrence of the device. The higher value of g_m will give proper amplification to the device. Another device parameter, g_{ds} i.e., the conductance at output, is inversely proportional to the intrinsic gain of the device. Variation in the ratio of drain current to the minimum change in drain voltage by maintaining constant voltage in gate defines the output conductance and mathematically expressed in equation 2.

$$g_{ds} = \left.\frac{\partial I_{DS}}{\partial V_{DS}}\right|_{V_{GS}=k} \quad (2)$$

In equation 1, and equation 2, *k* denotes a constant value. Figure 5 show the output-conductance plotted for the NADGNFET device. It can be seen that at strong inversion linear region, the g_{ds} is a large value proportional to the metal work function but in saturation the g_{ds} decreases which may increase the intrinsic gain of the device. From g_m and g_{ds} curves, it can be concluded that increasing overdrive voltage will decrease the gain from the devices when current is held constant [8]. The g_m and g_{ds} are the dominant source of non-linearity. At lower frequency, the g_m is nonlinearly dominant at lower load of impedance, but at high frequency operation the output-conductance is also a source of nonlinearity. The parasitic capacitances and the substrate system do not create significant nonlinearity, but they reduce output-conductance nonlinear behavior at high frequencies because capacitive shunt reduces the output-impedance and output voltage swing. The intrinsic gain is mathematically given by equation 3.

$$A_{VO} = \frac{g_m}{g_{ds}} \quad (3)$$

The intrinsic gain plot is shown in figure 6 for the device shown in figure 1. For nanoscale application, the NADGNFET is best suitable because of the maximum intrinsic gain A_{VO} = 19 V/V at moderate inversion and a gradual decrease in saturation region. As current remains constant in the saturation region, it decreases to lower values for channel length modulation and drain induced barrier lowering. For analog circuit, there must be low output conductance for acquiring good intrinsic gain values. Values of obtained FOM are compared in table 1.

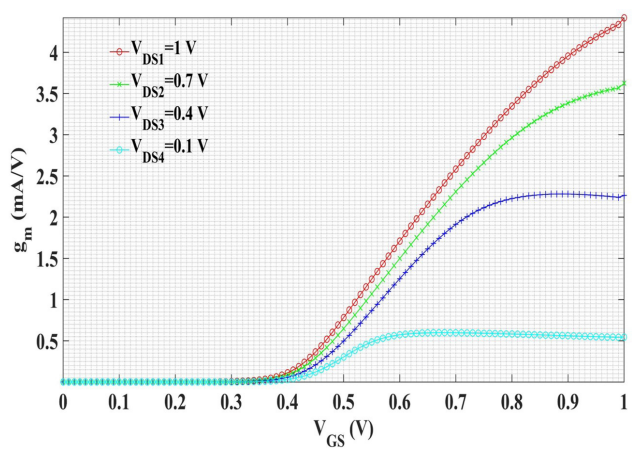


Figure 4: The transconductance plot of the NADGNFET device.

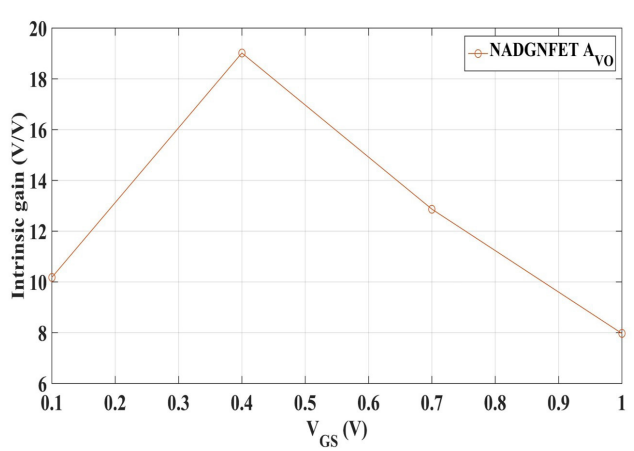


Figure 6: The intrinsic gain plot of NADGNFET device.

Table 1: A comparison of proposed device with past works.

Devices	L_G (nm)	V_{TH} (V)	DIBL (mV/V)	SS (mV/dec)	f_T (THz)	I_{ON} (Amp)	I_{ON}/I_{OFF}
Multi FinFET [12]	30	0.29	-	83.5	-	1.04×10^{-8}	7.7×10^{5}
n^+ Pocket AJ-JL MOSFET [13]	20	0.5	13.4	59	-	127×10^{-6}	1×10^{13}
Si Nanotube FET [14]	20	0.3	63.15	72	-	-	1×10^{5}
Proposed 3D-NADGNFET	40	0.38	18.5	59	3.4	1.46×10^{-3}	2.1×10^{8}

Note: All the devices reported in this table were biased with supply voltage = 1 V.

Results and Discussion

The RF and linearity FOM

This section analyses the device RF and linearity properties under different test condition giving a detailed performance by the NADGNFET device. It is important to analyze the RF/linearity as the device may be operated at high frequency range [9]. The short circuit current gain reaches unity for frequency is known as the cut-off frequency (f_T) in the RF circuits. It gives a difference between bandwidth and power; it is used for average to very speed design. Mathematically, the f_T is given by the equation 4, the f_T is dependent on the parameter g_m, and total gate capacitance $C_{GG} = C_{GS} + C_{GD}$, where C_{GS}, and C_{GD}, are gate to source, and gate to drain capacitance, respectively.

$$f_T = \frac{g_m}{2\pi C_{GG}} \tag{4}$$

The f_T versus gate bias voltage is plotted as shown in figure 7, for a fixed value of V_{DS} = 1 V for the NADGNFET device. The cut-frequency for the NADGNFET device was plotted using the extracted g_m and C_{GG} data (figure 7), for a gate-source voltage range of 0 - 1 V at V_{DS} = 1 V. The plot shows that the f_T rises after subthreshold and reaches a maximum value of 3.4 THz in strong inversion.

The mathematical expressions of another important parameters i.e., TGF and TFP, are defined by equation 5 and equation 6, respectively.

$$TGF = \frac{g_m}{I_{DS}} \tag{5}$$

$$TFP = \frac{g_m}{I_{DS}} \times f_T \tag{6}$$

The TGF is plotted in figure 8, it helps to determine the device small signal efficiency, it gives highest peak = 34 V^{-1} at weak inversion and reduces in the strong inversion region. This behavior of the proposed device is similar to nano-scale MOSFET device. The peak TFP value is 15.83 THz/V for the NADGNFET device. The obtained parameters range is suitable for the high frequency range applications. The GFP and GTFP is given by equation 7 and equation 8, respectively.

$$GFP = A_{VO} \times f_T \tag{7}$$

$$GTFP = A_{VO} \times TFP \tag{8}$$

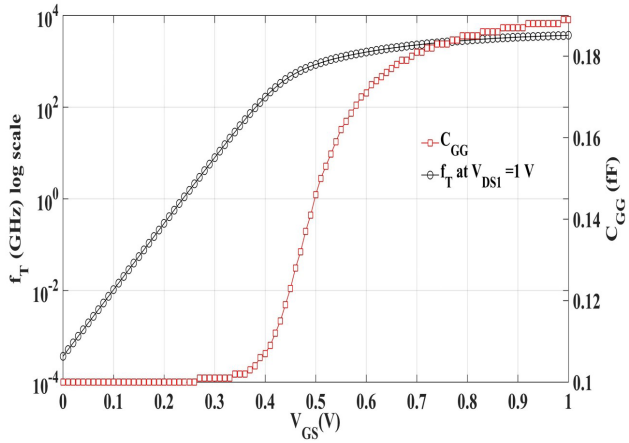


Figure 7: The cut-off and total gate capacitance plot of the NADGNFET device.

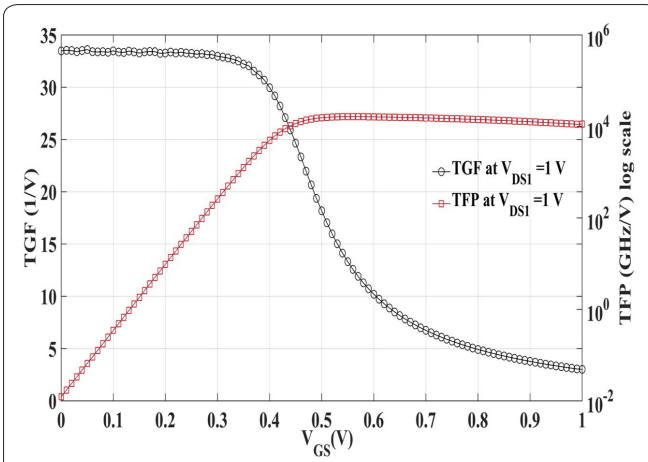


Figure 8: The TGF and TFP plot of NADGNFET device.

GFP and GTFP are the important parameters to evaluate the device RF performance. As shown in figure 9, the GFP keeps up harmony among bandwidth and power in high-speed circuit design. The GTFP establishes the utmost operation region with transconductance, gain, and frequency. The GTFP is also required as amplifier to make it easy for high values of operating frequencies [10]. For the present device their values were 32.27 THz and 279.4 THz/V giving a large margin for device operation. The gate or transport delay is defined by equation 9.

$$\tau_m = C_{GG} \times \left(V_{DD}/I_{ON}\right) \tag{9}$$

Where V_{DD} = 1 V is the supply voltage.

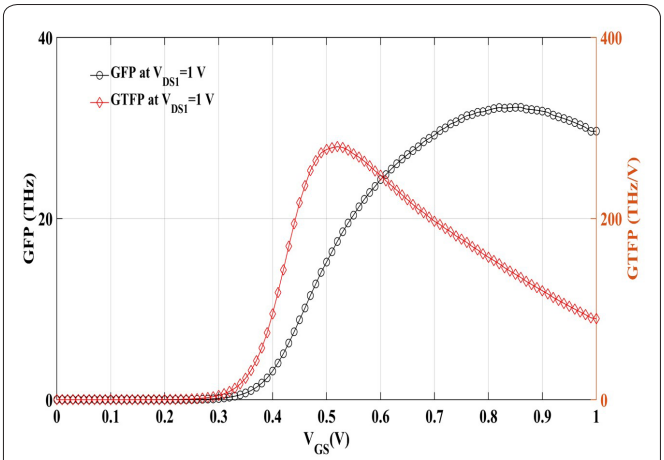


Figure 9: The GFP and GTFP plot for the NADGNFET device.

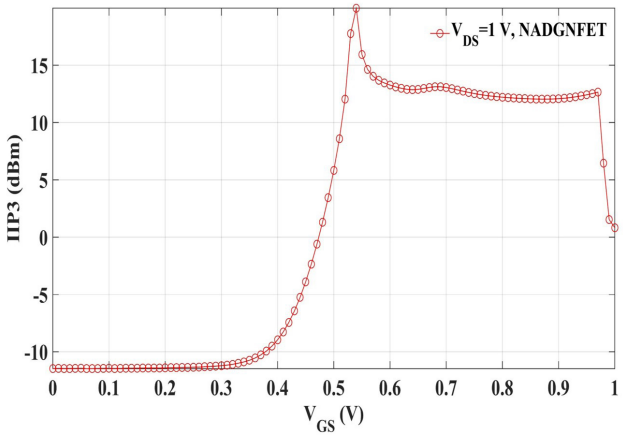


Figure 11: The IIP3 plot of NADGNFET device.

The variation in τ_m as a function of V_{GS} is plotted in figure 10. It is observed that the change in C_{GG} is negligible with respect to the change in I_{ON}. Hence, τ_m improves with the increase in V_{GS}, the value is 0.258 pico-sec. The measured RF values for the NADGNFET device shows that at the bulk implementation, it can maintain specification integrity with the advancement in the CMOS technology and can contribute a remarkable improvement in the high-frequency RF performance of the Integrated Circuits at silicon level applications.

The important linearity parameter in evaluating the low-level effect of intermodulation is the IIP3 [11], and is defined as the intersection of the third and first order harmonics. To calculate IIP3, the equation 10 is used and expressed in dBm i.e., equation 11.

$$IIP3 = 4 \text{ x } \frac{1}{R_{in}} \text{ x } \left| \frac{g_m}{g'_{m3}} \right| \tag{10}$$

$$IIP3(dBm) = 10 \text{ x } \log_{10}(1000 \text{ x } IIP3) \tag{11}$$

For a good linear response, the IIP3 value should be higher in strong inversion. The IIP3 is plotted in figure 11 for the proposed device, the plot depicts a peak value of IIP3 in strong inversion greater than 10 dBm, hence the device will give power to the applied RF signals with low harmonics. The IMD3 is the ratio of third and first-order intermodulation harmonics. The IMD3 is essential to evaluate the presence of distortion when double tone frequencies given to the nanodevice [11]. The P_{out} with A = 1 V (peak value), and R_L (resistance load) = 50 Ω, is given by equation 12.

$$P_{OUT} = \frac{g_m^2}{R_L} \text{ x } A^2 \tag{12}$$

The mathematical expression of IMD3 is given by equation 14 based on Output Intercept Power Point-3 (OIP3) defined by equation 13.

$$OIP3(dBm) = \log_{10}(g_m^2) + IIP3(dBm) \tag{13}$$

$$IMD3(dBm) = 3 \text{ x } P_{OUT}(dBm) - 2 \text{ x } OIP3(dBm) \tag{14}$$

The IMD3 is plotted in figure 12, in strong inversion, the IMD3 value is: -120 dBm, which is a low value, hence the device will present low distortion at the RF frequencies. Table 1 shows the comparison of the present device with past works, the comparison shows the NADGNFET device has achieved better parameter value on the wide FOM performance scale.

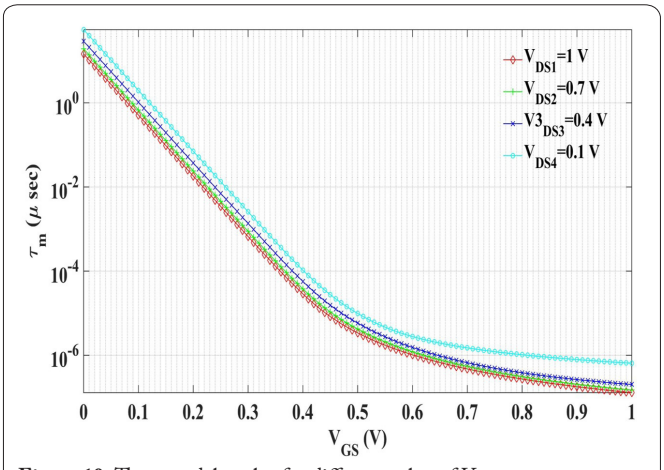


Figure 10: The gate delay plot for different value of V_{DS}.

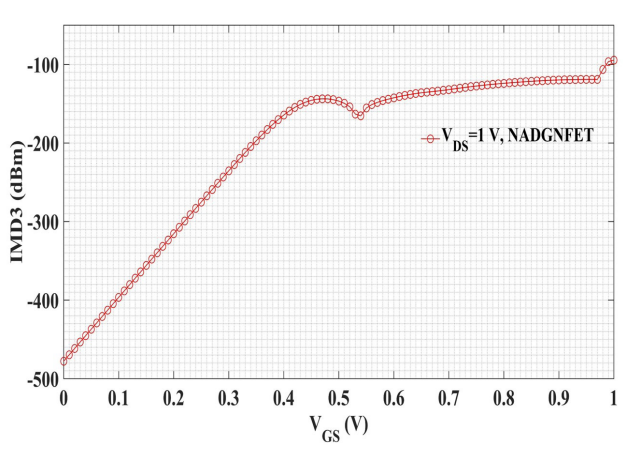


Figure 12: A IMD3 plot of NADGNFET device.

Conclusion

The analog, RF and linearity figures of merit of the proposed non-aligned DG n-channel MOSFET with HfO_2 as gate dielectric material has been investigated and presented in detail. The results show the device performs well in every FOM scale. The presented device was also compared with past works and has given improved parameter values, making it better for low power and high frequency applications.

Acknowledgments

Authors expresses their gratitude to VIT-AP University (Andhra Pradesh, India) management to help extended to this work.

Conflict of Interest

None.

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