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Short Communication

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Wire-Based Core Field Effect Transistor (CoreFET)

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Abstract

We report a novel proof-of-concept FET design (CoreFET) based on a thin wire, which can be fabricated without any micromanufacturing processes. Zinc oxide (ZnO) and Poly(3-hexylthiophene) (P3HT) were used to develop thin film CoreFETs, with the central core of a wire acting as a gate terminal. The design may be used for multiple electronic and optoelectronic devices, and the unique wire shape renders it favorable for specific applications, such as chemical and biological sensing.

Keywords

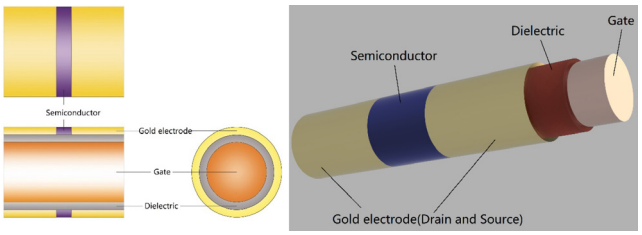
CoreFET, Field-effect transistors, Thin film transistors

Introduction

Field-effect transistors (FET) have been widely used in microelectronic devices, from the basis for modern digital integrated circuits [1] to combustion engine ignition coils [2]. Different implementations of FETs have been developed. The early common ones are junction field-effect transistors (JFETs) [3], metal-oxide-semiconductor field effect transistors (MOSFETs) [4], etc.; newly-added FETs include carbon nanotube field effect transistors (CNTFETs) [5, 6], organic field effect transistors (OFETs) [7], etc. In an FET, a gate voltage generates an electric field in the device and regulates the conductivity of a semiconductor body between the source and drain. Since the gate geometry plays an important role in enhancing the performance of FET devices, there has been great interest in the development of device architecture. For example, the conventional planar back gate MOSFETs evolved into a double gate to trigate MOSFETs [8].

Thin film transistors (TFTs) are generally made up of a geometry with a bottom gate and a top drain/source. Studies on modulating TFTs by changing gate texture [9] and curvature [10] have also been reported. Most of the existing FETs are fabricated using micromanufacturing processes that are time-consuming and expensive. Assembling a FET device without a micromanufacturing process will make it more approachable to researchers in other fields. In this short communication, we report a novel proof-of-concept FET design based on a thin wire design (Scheme 1), which can be fabricated without any micromanufacturing processes. The term CoreFET is used due to the structure and design of the device. The design and the unique wire shape render it favorable for specific applications in multiple flexible electronic and optoelectronic devices, such as chemical and biological sensors.

A FET typically has three terminals: source, drain, and gate. The schematic design of our CoreFET is shown in Scheme 1. In this device, the core of a



Scheme 1: Schematic of a CoreFET structure.

metal wire acts as a gate terminal, which is covered with a thin film of dielectric material - either SiO_2 or polyethylene glycol terephthalate (PGT) in our experiments. A thin film of a semiconductive material is coated on the dielectric materials, and this semiconductor body is connected with source (S) and drain (D) terminals. A current flows through the semiconductor body from the source to the drain terminals.

Since FETs are commonly used as amplifiers, we expect that the electron flow or current between the source and drain is influenced by the applied gate voltage. This device may particularly be useful for making chemical or biological sensors, such as chemical field effect transistor sensing. First, the semiconductive sensing material is exposed to the outside environment. Second, the thin wire design allows the device to be used for detecting chemicals in a small volume, such as in living cells.

A variety of semiconductors can be used to prepare FETs. While single crystalline silicon is most common, covering a layer of single crystalline silicon on a wire is quite challenging. Instead, we applied zine oxide (ZnO) and Poly(3-hexylthiophene) (P3HT) to develop thin film CoreFETs in our proof-of-concept studies since both have been studied in other FET designs. The two compounds represent an inorganic and an organic material, respectively.

Materials

ZnO and P3HT were used as the two semiconductor materials in this work. For a P3HT CoreFET device (Figure 1), an enameled copper wire was used as the core wire and the enameled PGT polymer layer was the dielectric material. P3HT (Alfa Aesar, Haverhill, MA) was used as purchased. The P3HT solution was prepared by dissolving 50 mg P3HT in 1 mL chloroform. Then the solution was spray-coated on a wire. The diameter of the wire was 50 mm and the thickness of the insulator was 10 mm. The channel length was 1 mm, and the channel width was the perimeter of the wire i.e., 0.314 mm.

Each ZnO CoreFET device (Figure 2) was produced and tested using a thin, glass insulated copper wire (GW Lab, Canoga Park, CA) as the core wire. The thin glass wire was preheated to 900 °C for 1 h in an attempt to fuse the glass coating before depositing a ZnO film. In deposition of ZnO films, a 0.2 M solution of $Zn(OAc)_2$ in isopropanol with small amount of monoethanolamine was spray-coated onto the thin glass insulated copper wire five times with the sprayer nozzle approximately 2 inches from the wire. The wire was then heated to 500 °C with a heating rate of 10 °C per minute and kept at 500 °C for 2 hours before cooling in an oven at a slow rate.

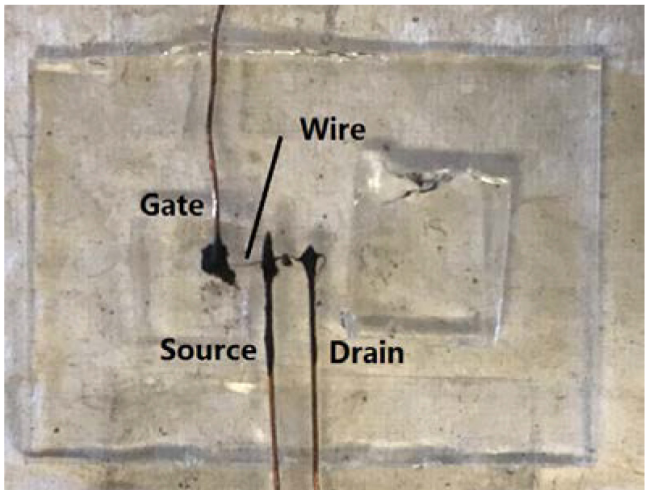


Figure 1: A P3HT CoreFET device made of a thin film of P3HT that was spray-coated on source and drain electrodes on an enameled copper wire.

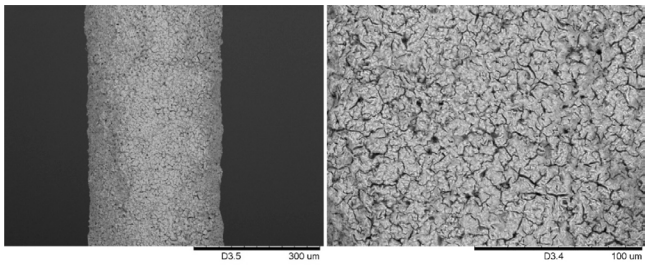


Figure 2: SEM images of a ZnO/glass/Cu wire. The right is a zoomed-in image showing cracks and pinholes in the ZnO film.

Results and Discussions

Our results showed that both devices presented FET behaviors (Figures 3 and 4). Figure 3 shows the source-drain current versus the source-drain voltage (I-V) of ZnO-modified CoreFET for different gate potentials.

ZnO is a known n-type semiconductor [11]. When a negative gate voltage is applied, it causes a depleting region in the ZnO coating near SiO_2, narrowing the conductive channel and resulting in a decrease in current. Therefore, changing the gate voltage alters the ZnO resistance. In the tested voltage range, the ZnO operates like a variable resistor in an ohmic mode. Larger drain-to-source voltage did not reach the saturation mode but showed an error message, which may be because of the cracks and pinholes in the SiO_2 coating (Figure 2). Further improvement and optimization of the device is necessary in future studies.

Figure 4 shows the FET behavior of a P3HT modified CoreFET. P3HT is a known p-type semiconductor [12]. A negative gate voltage applied to P3HT body attracts the positively charged holes within the body towards the gate. This forms a more conductive channel in the P3HT coating near the dielectric coating, increasing the current as a result (Figure 4).

In conclusion, we presented two examples of a novel CoreFET design, in which the central core of a wire acts

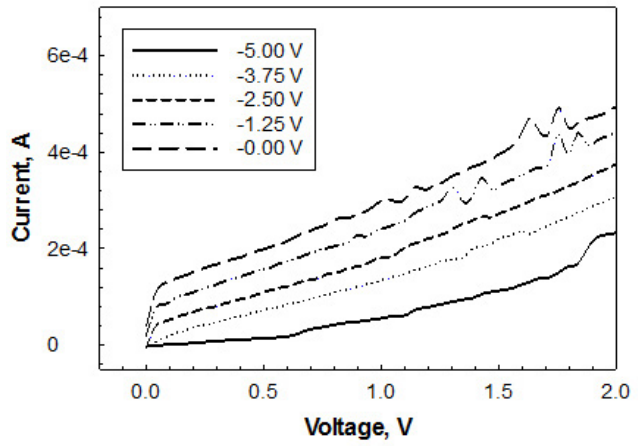


Figure 3: Output characteristics of a ZnO coated CoreFET.

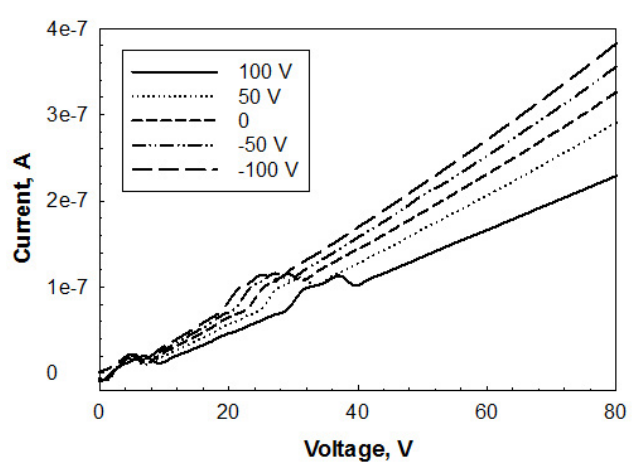


Figure 4: Output characteristics of a P3HT coated CoreFET.

as a gate terminal. The two semi-conductive materials used include n-type ZnO and p-type P3HT. The designs may find various applications within chemical and biological sensing, which will be studied in the near future. The electron flow from the source to drain will be affected by the gate voltage applied across the gate and source terminals, the length and thickness of the semi-conductive coating, the material and the thickness of the dielectric layer, the uniformity of the coatings, etc. Given that these factors have an effect on the performance of the CoreFETs, they will be optimized to achieve the best possible results in future studies.

Acknowledgements

K.C. and H.-F.J. conceived and designed the experiments; K. C., Z. Q., T. M., and J. K. performed the experiments and analyzed the data; All authors have contributed in writing the paper.

Conflict of Interest

The authors declare that they have no conflicts of interest.

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